



CURRICULUM
for
POST-GRADUATE DEGREE PROGRAM

MASTER OF TECHNOLOGY
IN

VLSI Design and Systems

Scheme of Teaching and Evaluation 2024

Outcome Based Education (OBE) and Choice Based Credit System (CBCS)
(Effective from the academic year 2024-25)

**In accordance with NEP 2020 and AICTE Model
Curriculum**



GRAPHIC ERA (DEEMED TO BE UNIVERSITY)

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1. Preamble

The role of higher education is very important in securing gainful employment and/or providing further access to higher education comparable to the best available in world-class institutions elsewhere. The improvement in the quality of higher education, therefore, deserves to be given the highest priority to enable the young generation of students to acquire skills, training and knowledge to enhance their thinking, comprehension, and application abilities and prepare them to compete, succeed and excel globally. Sustained initiatives are required to reform the present higher education system to improve and upgrade the academic resources and learning environments by raising the quality of teaching and standards of achievement in learning outcomes in undergraduate programs. The Graphic Era (Deemed to be University) upgraded its undergraduate programmes in Electronics and Communication Engineering in accordance with the model curriculum proposed by AICTE and guidelines of NEP, 2020 including Outcome Based Education (OBE) and Choice Based Credit System (CBCS), which makes it student-centric, interactive with well-defined aims, objectives, and goals. NEP, 2020 aims at making higher education a multidisciplinary learning process. In other words, the curriculum will be flexible, it will allow students to take up creative subject combinations.

2. About the Department

The Department of Electronics and Communication Engineering was established in the year 2001. The motive of the department is to imparting knowledge in cutting-edge technologies. Initially department started under-graduate programme and gradually started postgraduate, Ph.D program. The department has experienced and well qualified faculty. Faculty members are actively involved in research activities and have many research publications in preferred *journals of high repute and have granted patents*. Faculty members also have undertaken sponsored research projects. In consonance with the rapidly evolving technology, specialized laboratories have been established in a view to strengthening research & development and industry demands. This gives our students a holistic and pragmatic view of the present scenario of the industry, and prepares them for a successful career in the field of Electronics and Communication Engineering. The department has signed several MoUs with reputed organizations and Universities for academic, research & industry collaborations.

3. Vision & Mission

3.1 Vision and Mission of the University

Vision

We visualize Graphic Era (Deemed to be University) as an internationally recognized, enquiry-driven, ethically engaged diverse community, whose members work collaboratively for positive transformation in the world, through leadership in teaching, research, and social action.

Mission

The mission of the university is to promote learning in true spirit and offering knowledge and skills in order to succeed as professionals. The university aims to distinguish itself as a diverse, socially responsible learning community with a high quality scholarship and academic rigor.

3.2 Vision and Mission of the Department

Vision

The Department visualizes itself to become leading centre of learning in the field of Electronics & Communication Engineering with academic excellence in research to produce self-motivated, creative, and socially responsible engineers and specialists, ready to take up challenges of industrial development with ethics and societal commitment.

Mission

M1: To provide high quality contemporary education in the field of Electronics & Communication Engineering and professional ethics to its learners.

M2: To provide creative learning environment for the students to equip them with strong foundation for continuing higher education.

M3: To pursue research and develop insight knowledge of current and emerging technologies in Electronics & Communication Engineering to serve the needs of the society, industry, and scientific community.

M4: To prepare students to have creative and innovative thinking to develop them into socially responsible professionals.

4. Program Educational Objectives

PEO1: Implementation of core-engineering knowledge to solve practical problems in the areas of VLSI design and Systems, and to produce innovative systems in these domains.

PEO2: Motivating entrepreneurship in VLSI domains by integration of sustainability with efficiently designed systems.

PEO3: Sharpening the educational, and research-oriented skills of the students for their easy merger into a future career in research or academia.

PEO4: Developing design engineers with excellent ability to communicate, along with a morally responsible behavior.

5. Consistency of PEOs with Mission of the Department:

PEO Statements	M1	M2	M3	M4
PEO 1	3	1	3	2
PEO 2	2	3	3	3
PEO 3	3	3	2	1
PEO 4	1	2	2	2

High correlation (3); Medium correlation (2); Low correlation (1), (-) No correlation

6. Program Outcomes (POs)

PO1. Apply the knowledge of science, mathematics, and engineering principles for developing problem solving attitude.

PO2. Identify, formulate, and solve engineering problems in the broad areas like System Design using VLSI.

PO3. Use different modern engineering software tools in the domain of VLSI and Systems Design.

PO4. Design and conduct experiments, analyze and interpret data, imbibe programming skills for development of simulation experiments.

PO5. Function as a member of a multidisciplinary team with sense of ethics, integrity, and social responsibility.

PO6. Realize the need for self-education and ability for independent and life-long learning.

7. Program Specific Outcomes (PSOs)

PSO1: Attain competency in areas of IC designing, testing, and developing prototype of various VLSI circuits.

PSO2: Integrating various VLSI sub-systems to design industrial circuits.

PSO3: Students gain skills in developing various complicated circuits and excel in industrial sector.

8. Program Structure

A. Definition of Credit:

<i>1 Hr. Lecture (L) per week</i>	<i>1 credit</i>
<i>1 Hr. Tutorial (T) per week</i>	<i>1 credit</i>
<i>1 Hr. Practical (P) per week</i>	<i>0.5 credit</i>
<i>2 Hours Practical (P) per week</i>	<i>1 credit</i>

B. Nomenclature as per AICTE

Course code	Definitions
L	Lecture
T	Tutorial
P	Practical
C	Credits
HSMC	Humanities and Social Sciences including Management courses
PCC	Professional Core Courses
BSC	Basic Science Courses
ESC	Engineering Science Courses
PEC	Professional Elective Courses
OEC	Open Electives Courses
LC	Laboratory courses
MC	Mandatory Courses
PROJ	Project/Seminar/Internship/Summer training

C. Nomenclature as per NEP 2020

Code	Definitions
DSC	Discipline Specific Courses
DSE	Discipline Specific Elective
UOE	University Open Elective
AEC	Ability Enhancement Courses
PROJ	Project/Seminar/Internship/Summer training
SEC	Skill Enhancement Courses

Definitions

Courses of study – Courses of study indicates pursuance of study in a particular discipline. Every discipline shall offer various categories of courses of study, viz. Discipline Specific Courses (DSC), Discipline Specific Electives (DSE), University Open Elective/Generic Elective (UOE) / Generic Elective (GE), Ability Enhancement Courses (AEC), Skill Enhancement Courses (SEC), Value Added Courses (VAC), Internship/Apprenticeship/Project/Community Outreach (PROJ) and Mandatory Non-Graded Course (MNG)

a) Discipline Specific Courses (DSC): Discipline Specific Courses is a course of study, which should be pursued by a student as a major component, of the discipline as mandatory requirement of his/her programme of study. DSC shall be the core credit courses of that particular discipline which will be appropriately graded and arranged across the semesters of study.

b) Discipline Specific Elective (DSE): The Discipline Specific Electives (DSE) shall be a pool of credit courses of that particular discipline (single discipline programme of study) or those disciplines (multidisciplinary programme of study), as the case may be, which a student chooses to study from his/her particular discipline(s). There shall be a pool of DSE from which a student may choose a course of study.

c) University Open Elective/Generic Elective (UOE/GE): An elective course chosen generally from other discipline(s) with an intention to seek exposure is called a University Open Elective/Generic Elective. UOE shall consist of a pool of courses offered by various disciplines of study in groups of odd and even semesters, from which a student can choose.

d) Ability Enhancement Courses (AEC): Ability Enhancement courses aim at enabling the students to acquire and demonstrate the core linguistic skills, including critical reading and expository and academic writing skills, that help students articulate their arguments and present their thinking clearly and coherently and recognize the importance of language as a mediator of knowledge and identity.

e) Skill Enhancement Courses (SEC): SE courses are skill-based courses in all disciplines and are aimed at providing hands-on-training, skills.

f) Value Addition Course (VAC): VA courses are value-based courses which are meant to inculcate ethics, culture, Indian Knowledge systems, constitutional values, soft skills, sports education and such similar values to students which will help in all round development of students.

g) Major Project/Seminar/Internship/Summer training (PROJ):

- i. Internship /Apprenticeship: All students will also undergo internships / Apprenticeships in a firm, industry, or organization or Training in labs with faculty and researchers in their own or other HEIs/research institutions.
- ii. Major Project: Students are required to take up major project under the guidance of a faculty member. The student shall be encouraged to get engaged in Research Based Project in final year (III and IV semesters). The research outcomes of their project work may be published in peer-reviewed journals or may be presented in conferences /seminars or may be patented.

9. Major Features of Curriculum

- A flexible choice-based system that enables students to pursue courses that align with their interests.
- Offering a number of courses to meet all of the VLSI Design and Systems requirements.
- The curriculum is structured to provide a balanced combination of academia, research and industry-relevant subjects that are taught through collaborative learning.
- Core courses establish a solid foundation in the development of front-end and back-end integrated circuits.
- This programme curriculum provides students with exposure to a variety of design software. Additionally, they acquire the ability to develop, simulate, implement, and evaluate sophisticated digital systems.
- High Practical approach through Project work and emerging technologies in VLSI and Wireless Communication courses in which students will visit the reputed research organizations and / or industries and perform real time project.
- To impart high competency in the students, the curriculum offers distinct ability enhancement and value-added courses.
- Apart from the technical course, the program offers a range of courses that provides the students a broad range of knowledge and skill set like life skills and mentoring, soft skills, Aptitude, Communication skills, social and professional ethics in engineering, environmental engineering, and management.



- The curriculum offers multi-disciplinary courses running in the university for other filed/areas.

Course Components of Academic Program M.Tech (VLSI Design and Systems)

Program Duration : 4 Semesters (2 Years)

S.No.	AICTE Course Components	Breakup of Credits
1.	Humanities and Social Sciences including Management courses (HSMC)	2
2.	Engineering Science courses including workshop, drawing, basics of electronics/electrical/mechanical/computer etc. (ESC)	5
3.	Professional Core Courses (PCC)	27
4.	Laboratory courses (LC)	10
5.	Professional Elective Courses (PEC)	9
6.	Project work, seminar and internship in industry or elsewhere (PROJ)	27
	Total Credits	80

S. No.	NEP Course Components	Breakup of Credits
1	Discipline Specific Courses (DSC)	37
2	Discipline Specific Elective (DSE)	9
3	Ability Enhancement Courses (AEC)	2
4	Skill Enhancement Courses (SEC)	5
5	Project/Seminar/Internship/Summer training (PROJ)	27
	Total Credits	80



10. Scheme



Graphic Era (Deemed to be University)
M. Tech (VLSI Design and Systems)
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Outcome Based Education (OBE) and Choice Based Credit System (CBCS) as per NEP 2020 and AICTE Model Curriculum
 (Effective from the academic year 2024-25)

Semester I

Course Module						Teaching Periods				Weightage: Evaluation			
COURSE													
S. No.	Code	Course title	NEP Component	AICTE Component	Credits	L	T	P	Contact Hr.	CIE	MSE	ESE	Total
1	VDM 101	Semiconductor Materials and Devices	DSC	PCC	3	3	0	0	3	25	25	50	100
2	VDM 102	CMOS Analog Circuit Design	DSC	PCC	3	3	0	0	3	25	25	50	100
3	VDM 103	Advanced Digital Integrated Circuit	DSC	PCC	3	3	0	0	3	25	25	50	100
4	VDM 104	VLSI Technology	DSC	PCC	3	3	0	0	3	25	25	50	100
5	VDM 14X	Program Elective-I	DSE	PEC	3	3	0	0	3	25	25	50	100
Laboratory and Others													
6	VDM 151	CMOS Analog Circuit Design Lab	DSC	LC	2	0	0	4	4	25	25	50	100
7	VDM 152	Digital VLSI Circuit Design Lab	DSC	LC	2	0	0	4	4	25	25	50	100
TOTAL					19	15	00	08	23	175	175	350	700



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Semester II

		Course Module				Teaching Periods				Weightage: Evaluation			
		COURSE											
S. No.	Code	Course title	NEP Component	AICTE Component	Credits	L	T	P	Contact Hr.	CIE	MSE	ESE	Total
1	VDM 201	Advanced ASIC and FPGA Design	DSC	PCC	3	3	0	0	3	25	25	50	100
2	VDM 202	Digital System Design using Verilog HDL	DSC	PCC	3	3	0	0	3	25	25	50	100
3	VDM 203	Advanced VLSI Circuit Testing	DSC	PCC	3	3	0	0	3	25	25	50	100
4	VDM 204	Low Power VLSI Design	DSC	PCC	3	3	0	0	3	25	25	50	100
5	VDM 24X	Program Elective-II	DSE	PEC	3	3	0	0	3	25	25	50	100
Laboratory and Others													
6	VDM 251	Verilog HDL Lab	DSC	LC	2	0	0	4	4	25	25	50	100
7	VDM 252	VLSI Physical Design Lab	DSC	LC	2	0	0	4	4	25	25	50	100
8	VDM 253	Mini Project with Seminar	PROJ	PROJ	1	0	0	2	2	25	0	75	100
9	GP201	General Proficiency	AEC	HSMC	1	0	0	0	-	100	-	-	100
TOTAL					21	15	00	10	25	300	175	425	900



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Semester III

		Course Module				Teaching Periods				Weightage: Evaluation			
		COURSE											
S. No.	Code	Course title	NEP Component	AICTE Component	Credits	L	T	P	Contact Hr.	CIE	MSE	ESE	Total
1	VDM 34X	Program Elective-III	DSE	PEC	3	3	0	0	3	25	25	50	100
2	VDM 301	VLSI Physical Design Automation	DSC	PCC	3	3	0	0	3	25	25	50	100
3	VDM 302	Research Methodology and IPR	SEC	ESC	2	2	0	0	2	25	25	50	100
	VDM 30X	Through Swayam	SEC	ESC	3	3	0	0	3	25	25	50	100
Laboratory and Others													
4	VDM 351	Modelling and Simulation Lab	DSC	LC	2	0	0	4	4	25	25	50	100
5	VDM 352	Dissertation Phase-I*	PROJ	PROJ	10	0	0	20	20	25	50	125	200
TOTAL					23	11	00	24	35	150	175	375	700

Skill Enhancement Course (SEC)- Through Swayam

Course Code	Course Name
VDM 303	C-Based VLSI Design
VDM 304	Introduction to Algorithms and Analysis
VDM 305	Introduction to Machine Learning



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*M. Tech (VLSI Design and Systems)***Scheme of Teaching and Evaluation 2024**Outcome Based Education (OBE) and Choice Based Credit System (CBCS) as per NEP 2020 and AICTE Model Curriculum
(Effective from the academic year 2024-25)***Semester IV***

			COURSE			Teaching Periods				Weightage: Evaluation			
S. No.	Code	Course title	NEP Component	AICTE Component	Credits	L	T	P	Contact Hr.	CIE	MSE	ESE	Total
1	VDM 401	Dissertation Phase-II	PROJ	PROJ	16	0	0	32	32	50	100	250	400
2	GP 401	General Proficiency	AEC	HSMC	1	0	0	0	-	100	-	-	100
TOTAL					17	00	00	32	32	150	100	250	500

NOTE: General Proficiency shall be assessed based on the participation in NCC, NSS, Research paper Publication (Journal/ Conference), Organizing events, competitions (Inter University, State, National, International level) including Music, Debate, Sports, Hackathon and so on.

List of all the courses offered in the curriculum under each of the components

List of courses offered under Discipline Specific Elective (DSE)

Sl. No.	Semester	Course Code	Course Name	Credits
1.	I	VDM 141	Advanced Nanotechnology	3
2.	I	VDM 142	Optimization Techniques in VLSI Design	3
3.	I	VDM 143	Theory and Application of Embedded Systems	3
4.	I	VDM 144	Digital Signal Processing for VLSI	3
5.	II	VDM 241	Micro-Sensors and MEMS	3
6.	II	VDM 242	RF Integrated Circuits	3
7.	II	VDM 243	VLSI Circuits for Biomedical Application	3
8.	II	VDM 244	Microwave & MM-wave Integrated Circuits and Applications	3
9.	III	VDM 341	Organic Electronics Devices and Circuits	3
10.	III	VDM 342	Memory Design and Testing	3
11.	III	VDM 343	System on Chip Design and Testing	3
12.	III	VDM 344	Internet of Things	3

List of courses offered under Ability Enhancement (AEC)

Sl. No.	Semester	Course Code	Course Name	Credits
1.	II	GP 201	General Proficiency-I	1
2.	IV	GP 401	General Proficiency-II	1

List of courses offered under Skill Enhancement (SEC)

Sl. No.	Semester	Course Code	Course Name	Credits
1.	III	VDM 302	Research Methodology and IPR	2
2.	III (Through Swayam)	VDM 303	C-Based VLSI Design	3
		VDM 304	Introduction To Algorithms and Analysis	
		VDM 305	Introduction to Machine Learning	



11. Syllabus

GRAPHIC ERA (DEEMED TO BE UNIVERSITY), DEHRADUN

SEMESTER I

S. No.	Department of Electronics and Communication Engineering						
1.	Subject Code	VDM 101	Course Title		Semiconductor Materials and Devices		
2.	Contact Hours	L	3	T	0	P	0
3.	Examination Duration	Theory		3	Practical		0
4.	Relative Weight	CIE	25	MSE	25	ESE	50
5.	Credit	03					
6.	Semester	First					
7.	Category of Course	DSC/ PCC					
8.	Pre-requisite	Basic Electronics Engineering (TEC-101/201), Electronic Devices and Circuits (TEC-301)					

9.	Course Outcomes	<p>After completion of the course the students will be able to:</p> <p>CO1: Create basic understanding of semiconductor device physics.</p> <p>CO2: Evaluate two terminal MOS structure in terms of its electrical parameters.</p> <p>CO3: Analyse the three terminal MOS structure in terms of electrical potential and charge.</p> <p>CO4: Apply surface potential and charges in different regions of MOSFET operation.</p> <p>CO5: Understand the short channel and narrow channel effects.</p> <p>CO6: Implement the concepts of semiconductor device physics in developing real life applications.</p>
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10. Details of the Course

S. No.	Contents	Contact Hours
1.	Unit 1: Basics of Semiconductors: Semiconductor materials, Energy levels, Intrinsic and extrinsic semiconductor, Equilibrium in absence/presence of electric field.	8
2.	Unit 2: PN Junction Diode: Junction diode: PN junction, Tunnel diode, Quasi-fermi levels, Depletion width capacitance and its application in doping profile determination, I-V characteristics of narrow and wide base diodes and their equivalent circuits, Breakdown mechanisms, Small signal ac impedance.	10
3.	Unit 3: Two Terminal MOS Structure:	10

	Flat band voltage, Potential balance and charge balance, Effect of gate body voltage on surface condition, Accumulation, Depletion, Inversion, General analysis, Small signal capacitance.	
4.	Unit 4: Three Terminal MOS Structure: Contacting the inversion layer, Body effect, Different regions of operation, Pinch-off voltage.	7
5.	Unit 5: Four Terminal MOS Structure: Transistor regions of operation, Complete all-region model, Simplified all-region model, Models based on quasi fermi potential, Regions of inversion in terms of terminal voltage, Temperature effects, Breakdown, Enhancement mode, Depletion mode transistors.	10
	Total	45

11. Suggested Books

S. No.	Name of Authors/Books/Publishers	Edition	Year of Publication / Reprint
	Textbooks		
1.	Tsividis, Yannis, and Colin McAndrew, " Operation and Modelling of the MOS Transistor ", Oxford: Oxford University Press..	3 rd	2003
2.	S. Kang and Y. Leblebici, " CMOS Digital Integrated Circuits, Analysis and Design ", Tata McGraw-Hill.	3 rd	2003
	Reference Books		
1.	Adel S. Sedra, Kenneth C. Smith, " Microelectronic Circuits ", Oxford University Press	7 ^h	2014
2.	S. Salivahanan and S. Arivazhagan, " Digital Circuits and Design ", Oxford University Press,	5 th	2008
3.	Robert L. Boylestad and Louis Nashelsky, " Electronic Devices and Circuit Theory ", Prentice Hall of India (PHI).	9 th	2006

12.	Mode of Evaluation	Test / Quiz / Assignment / Mid Term Exam / End Term Exam
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GRAPHIC ERA (DEEMED TO BE UNIVERSITY), DEHRADUN

SEMESTER I

S. No.	Department of Electronics and Communication Engineering						
1.	Subject Code	VDM 102	Course Title		CMOS Analog Circuit Design		
2.	Contact Hours	L	3	T	0	P	0
3.	Examination Duration	Theory		3	Practical		0
4.	Relative Weight	CIE	25	MSE	25	ESE	50
5.	Credit	03					
6.	Semester	First					
7.	Category of Course	DSC/PCC					
8.	Pre-requisite	Electronics Devices and Circuits (TEC 301)					

9.	Course Outcomes	<p>After completion of the course the students will be able to:</p> <p>CO1: Recall the knowledge of analog IC design in CMOS technologies.</p> <p>CO2: Understand MOS transistors with different configurations.</p> <p>CO3: Apply the concepts of multistage and differential MOS amplifiers.</p> <p>CO4: Analyse the current mirror circuits.</p> <p>CO5: Assess the feedback amplifiers and phase locked loop.</p> <p>CO6: Design and develop various CMOS analog circuits.</p>
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10. Details of the Course

S. No.	Contents	Contact Hours
1.	Unit 1: Models for Integrated Circuit Active Devices: The depletion region of a PN junction, Depletion region capacitance and junction breakdown, Basics of MOS transistor, Derivation of current-voltage relationship, Analysis of MOS as an amplifier, Small signal models of MOS transistor, MOS transistor frequency response.	9
2.	Unit 2: Single Stage Amplifier: Common source stage with resistive load, CS stage with diode connected load, CS stage with current source load, CS stage with triode load, CS stage with source generation, Source follower and common gate configuration.	9
3.	Unit 3: Multistage Amplifier and Operational Amplifier: Cascode current source, Cascode amplifier, Differential pair, Small and large signal analysis of differential amplifier, Differential amplifier with MOS loads, OPAMP design: General consideration, Single stage OpAmp	9
4.	Unit 4: Current Mirrors, Active Loads and References:	9



	<i>Simple current mirror, Cascode current mirror, Wilson current mirror, Common source amplifier with complementary load, Voltage and current references: Widlar and peaking current sources, supply insensitive biasing</i>	
5.	Unit 5: Feedback and Non-Linear Analog Circuits: <i>General consideration, Properties of feedback circuits, Feedback configuration, Nonlinear analog circuits: LC oscillators, Simple phase locked loop.</i>	9
	Total	45

11. Suggested Books

S. No.	Name of Authors/Books/Publishers	Edition	Year of Publication / Reprint
	Textbooks		
1.	B. Razavi, “ Design of analog CMOS Integrated Circuits ”, McGraw-Hill	1 st	2002
2.	Mohammed Ismail and Terri Faiz, “ Analog VLSI Signal and Information Process ”, McGraw-Hill.	1 st	1994
	Reference Books		
1.	Paul R. Gray and R. G. Meyer, “ Analysis and Design of Analog Integrated Circuits ”, John Wiley and Sons	4 th	2001
2.	R. Jacob Baker, H. W. Li, and D.E. Boyce, “ CMOS: Circuit Design, Layout and Simulation ”, Prentice-Hall of India	3 rd	2010

12.	Mode of Evaluation	<i>Test / Quiz / Assignment / Mid Term Exam / End Term Exam</i>
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GRAPHIC ERA (DEEMED TO BE UNIVERSITY), DEHRADUN

SEMESTER I

S. No.	Department of Electronics and Communication Engineering						
1.	Subject Code	VDM 103	Course Title		Advanced Digital Integrated Circuit		
2.	Contact Hours	L	3	T	0	P	0
3.	Examination Duration	Theory		3	Practical		0
4.	Relative Weight	CIE	25	MSE	25	ESE	50
5.	Credit	03					
6.	Semester	First					
7.	Category of Course	DSC/PCC					
8.	Pre-requisite	Basic Electronics Engineering and Digital Electronics					

9.	Course Outcomes	<p>After completion of the course the students will be able to:</p> <p>CO1: Describe the basic MOS structure and layout design</p> <p>CO2: Understand the static and dynamic characteristics of MOS inverters</p> <p>CO3: Apply the MOS concepts to design combinational and sequential MOS logic circuits.</p> <p>CO4: Analyze different digital MOS logic circuits.</p> <p>CO5: Estimate power consumption of CMOS logic circuits.</p> <p>CO6: Integrate various concepts of digital VLSI circuit design and apply them in designing of MOS based digital circuits.</p>
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10. Details of the Course

S. No.	Contents	Contact Hours
1.	Unit 1: Introduction and Implementation of strategies for digital ICs: Issues in Digital Integrated Circuit Design, Quality Metrics of a Digital Design, Design rule: Stick diagram and layout. Custom Circuit design, Cell based, and Array based design implementations.	10
2.	Unit 2: MOS Inverters: Static and Dynamic Characteristics of CMOS inverter, Power dissipation, Logical effort.	8
3.	Unit 3: Designing combinational and sequential circuits: Static CMOS design, Different styles of logic circuits, Logical effort of complex gates, Static and dynamic properties of complex gates, Dynamic CMOS Logic. Timing metrics of sequential circuits, Dynamic latches and Registers. Pipelining.	10
4.	Unit 4: Interconnect and Timing Issues: Circuit characterization and performance estimation - Resistance, Capacitance estimation - Switching characteristics - Delay models –Timing	10



	<i>issues in Digital circuits, Power dissipation. Impact of Clock Skew and Jitter.</i>	
5.	Unit 5: Memory Design: <i>Read-Only Memories, ROM cells, Read-write memories (RAM), dynamic memory design, 6 transistor SRAM cell, Sense amplifiers</i>	7
	Total	45

11. Suggested Books

S. No.	Name of Authors/Books/Publishers	Edition	Year of Publication / Reprint
	Textbooks		
1.	S. Kang and Y. Leblebici, “ CMOS Digital Integrated Circuits, Analysis and Design ”, Tata McGraw-Hill.	3 rd	2003
2.	J. M. Rabaey, A. Chandrakasan and B. Nikolic, “ Digital Integrated Circuits: A Design Perspective ”, Prentice-Hall of India.	2 nd	2006
	Reference Books		
1.	John P. Uyemura, “ Introduction to VLSI Circuits ”, Wiley India Pvt. Ltd.	1 st	2012
2.	Eugene Fabricius, “ Introduction to VLSI Design ”, New Ed Edition, Tata McGraw - Hill Education.	1 st	1990
3.	N. H. E. Weste et. al., “ CMOS VLSI Design ”, Pearson.	3 rd	2005
4.	R. Jacob Baker, “ CMOS: circuit design, layout, and simulation ”, John Wiley & Sons	3 rd	2010

12.	Mode of Evaluation	<i>Test / Quiz / Assignment / Mid Term Exam / End Term Exam</i>
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GRAPHIC ERA (DEEMED TO BE UNIVERSITY), DEHRADUN

SEMESTER I

S. No.	Department of Electronics and Communication Engineering						
1.	Subject Code	VDM 104	Course Title		VLSI Technology		
2.	Contact Hours	L	3	T	0	P	0
3.	Examination Duration	Theory		3	Practical		0
4.	Relative Weight	CIE	25	MSE	25	ESE	50
5.	Credit	03					
6.	Semester	First					
7.	Category of Course	DSC/PCC					
8.	Pre-requisite	Basic Electronics Engineering and Digital Electronics					

9.	Course Outcomes	<p>After completion of the course the students will be able to:</p> <p>CO1: Explain about wafer fabrication techniques and oxidation process</p> <p>CO2: Analyse photolithography and etching techniques of VLSI design.</p> <p>CO3: Extend the knowledge of different physical and chemical deposition methods.</p> <p>CO4: Investigate metal deposition techniques and IC fabrication methodologies.</p> <p>CO5: Design and analysis of different packaging methods.</p> <p>CO6: Create a base for the semiconductor device fabrication using VLSI technology.</p>
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10. Details of the Course

S. No.	Contents	Contact Hours
1.	Unit 1: Wafer Preparation and Oxidation: Electron grade silicon, Crystal growth, Wafer preparation, Processing considerations, Vapor phase epitaxy and molecular beam epitaxy, Film characteristics, SOI structure, Oxide formation, Kinetics, Oxidation systems, Dry and wet oxidation, Masks properties of SiO ₂ , Oxidation defects, Redistribution of dopant at interface, Oxidation of poly silicon.	10
2.	Unit 2: Lithography and Etching: Optical, Electron, X-Ray and Ion Lithography methods, Positive and negative photo resist. Plasma properties, Size, Control, Etch mechanism, Etch techniques and equipment.	9
3.	Unit 3: Deposition and diffusion: Deposition process and methods, Diffusion in solids, Diffusion equation and Diffusion mechanisms, Flick's one-dimensional diffusion equation, Atomic diffusion mechanism, Measurement techniques, Range theory, Implant	10



	equipment, Ion implantation, Damage and annealing, Ion implantation systems.	
4.	Unit 4: Metallization and IC Fabrication: Metallization and its applications, Process simulation of Ion implementation, Diffusion, Oxidation, Epitaxy, Lithography, Etching and deposition, Annealing shallow junction – High energy implantation, Physical vapours deposition patterning. NMOS, CMOS and bipolar IC technologies and IC fabrication.	10
5.	Unit 5: Packaging: Analytical and assembly techniques and packaging of VLSI devices.	6
	Total	45

11. Suggested Books

S. No.	Name of Authors/Books/Publishers	Edition	Year of Publication / Reprint
	Textbooks		
1.	S. M. Sze, “ VLSI Technology ”, McGraw Hill.	2 nd	1988
2.	W. Wolf, “ Modern VLSI Design ”, Pearson	3 rd	2002
	Reference Books		
1.	S. K. Gandhi, “ VLSI Fabrication Principles Silicon and Gallium Arsenide ”, Wiley-INDIA	2 nd	1994
2.	Wai Kai Chen, “ VLSI Technology ”, CRC press	1 st	2003

12.	Mode of Evaluation	Test / Quiz / Assignment / Mid Term Exam / End Term Exam
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GRAPHIC ERA (DEEMED TO BE UNIVERSITY), DEHRADUN

SEMESTER I

S. No.	Department of Electronics and Communication Engineering						
1.	Subject Code	VDM 151	Course Title		CMOS Analog Circuit Design Lab		
2.	Contact Hours	L	0	T	0	P	4
3.	Examination Duration	Theory		0	Practical		4
4.	Relative Weight	CIE	25	MSE	25	ESE	50
5.	Credit	02					
6.	Semester	First					
7.	Category of Course	DSC/LC					
8.	Pre-requisite	Electronics Devices and Circuit, VLSI Technology and Design					

9.	Course Outcomes	<p>After completion of the course the students will be able to:</p> <p>CO1: Understand Cadence Virtuoso simulation tool for circuit implementation.</p> <p>CO2: Design Analog circuits, and operational amplifier using Cadence tool.</p> <p>CO3: Analyse various CMOS based circuits for layout and simulation using Cadence tool.</p> <p>CO4: Apply the acquired knowledge to develop CMOS based circuits.</p>
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10. Details of the Course

S. No.	List of problems for which student should develop program and execute in the Laboratory	Contact Hours
1.	Design, simulation and test to build common source amplifier using 90 nm technology in cadence tool.	2
2.	Create a layout of common source amplifier using 90 nm technology in cadence tool.	2
3.	Design, simulation and test to build common drain amplifier using 90 nm technology in cadence tool.	2
4.	Create a layout of common drain amplifier using 90 nm technology in cadence tool.	2
5.	Design, simulation and test to build differential amplifier using 90 nm technology in cadence tool.	2
6.	Create a layout of Differential amplifier using 90 nm technology in cadence tool.	2
7.	Design, simulation and test to build operational amplifier using 90 nm technology in cadence tool.	2



8.	Create a layout of operational Amplifier using 90 nm technology in cadence tool.	2
9.	Design, simulation and test to build Cascode amplifier using 90 nm technology in cadence tool.	2
10.	Create a layout of Cascode Amplifier using 90 nm technology in cadence tool.	2
11.	Design, simulation and test to build current mirror circuits using 90 nm technology in cadence tool.	2
12.	Create a layout of current mirror circuits using 90 nm technology in cadence tool.	2
Total		24
Innovative Experiments		
13.	Design and simulation of analog to digital converter using 90 nm technology in cadence tool.	2
14	Design and Simulation of widlar circuit using 90 nm technology in cadence tool.	2
Total		04

11. Suggested Books

S. No.	Name of Authors/Books/Publishers	Edition	Year of Publication / Reprint
	Textbooks		
1.	B. Razavi, “ Design of analog CMOS Integrated Circuits ”, McGraw-Hill	1 st	2002
2.	Paul R. Gray and R. G. Meyer, “ Analysis and Design of Analog Integrated Circuits ”, John Wiley and Sons	4 th	2001
3.	Mohammed Ismail and Terri Faiz, “ Analog VLSI Signal and Information Process ”, McGraw-Hill	1 st	1994
	Reference Books		
1.	R. Jacob Baker, H. W. Li, and D.E. Boyce, “ CMOS: Circuit Design, Layout and Simulation ”, Prentice-Hall of India.	3 rd	2010

12.	Mode of Evaluation	Test / Quiz / Assignment / Mid Term Exam / End Term Exam
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GRAPHIC ERA (DEEMED TO BE UNIVERSITY), DEHRADUN

SEMESTER I

S. No.	Department of Electronics and Communication Engineering						
1.	Subject Code	VDM 152	Course Title		Digital VLSI Circuit Design Lab		
2.	Contact Hours	L	0	T	0	P	4
3.	Examination Duration	Theory		0	Practical		4
4.	Relative Weight	CIE	25	MSE	25	ESE	50
5.	Credit	02					
6.	Semester	First					
7.	Category of Course	DSC/LC					
8.	Pre-requisite	Digital Electronics					

9.	Course Outcomes	<p>After completion of the course the students will be able to:</p> <p>CO1: Understand the CMOS based digital integrated circuits</p> <p>CO2: Analyze CMOS based combinational circuits using 45 nmTechnology</p> <p>CO3: Evaluate CMOS based sequential circuits and memory devices.</p> <p>CO4: Design and validate various CMOS based digital circuits using Cadence tool.</p>
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10. Details of the Course

S. No.	List of problems for which student should develop program and execute in the Laboratory	Contact Hours
1.	Design and comparison of DC and transient output characteristics of CMOS inverter at different aspect ratio.	2
2.	Draw a layout of CMOS inverter using 45 nm technology and check for LVS and DRC for inverter circuit.	2
3.	Design and implement various gates with CMOS logic along with its layout.	2
4.	Draw a schematic of carry look ahead adder using 45 nm technology and analyse its transient characteristics.	2
5.	Draw the layouts of carry look ahead adder using 45 nm technology and simulate its transient characteristics.	2
6.	Design a schematic of 2-bit comparator using 45 nm technology and simulate its transient characteristics	2
7.	Design and Implementation of 8:1 Multiplexer using 2:1 Multiplexer.	2
8.	Design the schematic of nand/nor latches/flip-flops using 45 nm technology and simulate its transient characteristics	2

9.	Design the schematic of universal counter using 45 nm technology and simulate its transient characteristics	2
10.	Design the schematic of ALU using 45 nm technology and simulate its transient characteristics	2
11.	Design the schematic of FSM (Moore's, Mealy Machines) using 45 nm technology and simulate its transient characteristics	2
12.	Design the schematic of 6T RAM using 45 nm technology and simulate its transient characteristics	2
	Total	24
Innovative Experiments		
13.	Design and implementation of Flash Memory with Cadence tool.	2
14.	Design and implementation of Different Analog to Digital converter (ADC) with Cadence tool.	2
15.	Simulate substrate bias (Body) effect in CMOS inverter.	2
	Total	06

11. Suggested Books

S. No.	Name of Authors/Books/Publishers	Edition	Year of Publication / Reprint
	Textbooks		
1.	S. Kang and Y. Leblebici, " CMOS Digital Integrated Circuits, Analysis and Design ", Tata McGraw-Hill.	3 rd	2003
2.	J. M. Rabaey, A. Chandrakasan and B. Nikolic, " Digital Integrated Circuits: A Design Perspective ", Prentice-Hall of India.	2 nd	2006
	Reference Books		
1.	John P. Uyemura, " Introduction to VLSI Circuits ", Wiley India Pvt. Ltd.	1 st	2012
2.	Eugene Fabricius, " Introduction to VLSI Design ", New Ed Edition, Tata McGraw - Hill Education.	1 st	1990
3.	N. H. E. Weste et. al., " CMOS VLSI Design ", Pearson.	3 rd	2005
4.	R. Jacob Baker, " CMOS: circuit design, layout, and simulation ", John Wiley & Sons,	3 rd	2010

12.	Mode of Evaluation	Test / Quiz / Assignment / Mid Term Exam / End Term Exam
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GRAPHIC ERA (DEEMED TO BE UNIVERSITY), DEHRADUN

SEMESTER II

S. No.	Department of Electronics and Communication Engineering						
1.	Subject Code	VDM 201	Course Title		Advanced ASIC and FPGA Design		
2.	Contact Hours	L	3	T	0	P	0
3.	Examination Duration	Theory		3	Practical		0
4.	Relative Weight	CIE	25	MSE	25	ESE	50
5.	Credit	03					
6.	Semester	Second					
7.	Category of Course	DSC/PCC					
8.	Pre-requisite	Advanced Digital Integrated Circuit					

9.	Course Outcomes	<p>After completion of the course the students will be able to:</p> <p>CO1: Describe the concepts of ASICs, CMOS Logic and ASIC Library Design.</p> <p>CO2: Understanding the concept of physical design of ASIC and FPGA.</p> <p>CO3: Analysis of different FPGA architecture and their performance comparison.</p> <p>CO4: Analysis of various trade-off in optimizing design for power, speed and area.</p> <p>CO5: Evaluation of speed, power and area of FPGA and ASIC based systems.</p> <p>CO6: Designing of ASIC, FPGA, SOC based systems using Xilinx family.</p>
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10. Details of the Course

S. No.	Contents	Contact Hours
1.	Unit 1: Introduction: Types of ASICs, Design flow, CMOS transistors CMOS design rules, Combinational logic cell, Sequential logic cell, Transistors as resistors, Transistor parasitic capacitance, Logical effort, Library cell design, Library architecture.	10
2.	Unit 2: ASIC Physical Design: System partition, partitioning, partitioning methods, interconnect delay models and measurement of delay, floor planning, placement, Routing, Circuit extraction, Design Rule Check.	9
3.	Unit 3: FPGA Architecture: Field Programmable gate arrays, Logic blocks, routing architecture, Design flow technology, Xilinx XC4000, ALTERA's FLEX 8000/10000,	10

	<i>ACTEL's ACT-1,2,3 and their speed performance Case studies: Altera MAX 5000 and 7000, Altera MAX 9000, Spartan II and Virtex II FPGAs.</i>	
4.	Unit 4: Trade off issues at System Level: <i>Optimization with regard to speed, area and power, asynchronous and low power system design. ASIC physical design issues, System Partitioning, Power Dissipation, Partitioning Methods.</i>	8
5.	Unit 5: System on Chip Design: <i>Design using Xilinx Family, System on Chip Design, SoC Design Flow, Platform based and IP based SoC designs, Basic Concept of Bus – Based communication architectures, On- chip communication architectures standards, Low power SoC designs.</i>	8
	Total	45

11. Suggested Books

S. No.	Name of Authors/Books/Publishers	Edition	Year of Publication / Reprint
	Textbooks		
1.	<i>Pasricha and N. Dutt, "On-Chip Communication Architectures System on Chip Interconnect", Elsevier.</i>	1 st	2008
2.	<i>Michael John Sebastian Smith, "Application-Specific Integrated Circuits", Addison-Wesley VLSI Systems Series</i>	1 st	2008
	Reference Books		
1.	<i>M. Rabaey, A. Chandrakasan, and B.Nikolic, "Digital Integrated Circuit Design Perspective", Wiley.</i>	2 nd	2003
2.	<i>Hoi-Jun Yoo, Kangmin Lee and Jun Kyong Kim, "Low-Power NoC for High-Performance SoC Design", CRC Press.</i>	1 st	2008

12.	Mode of Evaluation	<i>Test / Quiz / Assignment / Mid Term Exam / End Term Exam</i>
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GRAPHIC ERA (DEEMED TO BE UNIVERSITY), DEHRADUN

SEMESTER II

S. No.	Department of Electronics and Communication Engineering						
1.	Subject Code	VDM 202	Course Title		Digital System Design using Verilog HDL		
2.	Contact Hours	L	3	T	0	P	0
3.	Examination Duration	Theory		3	Practical		0
4.	Relative Weight	CIE	25	MSE	25	ESE	50
5.	Credit	03					
6.	Semester	Second					
7.	Category of Course	DSC/PCC					
8.	Pre-requisite	Digital Electronics					

9.	Course Outcomes	<p>After completion of the course the students will be able to:</p> <p>CO1: Describe digital circuits and its implementation through Verilog HDL code.</p> <p>CO2: Understand the concept of logic synthesis using Verilog HDL, and its impact in verification.</p> <p>CO3: Design various combinational and sequential circuits.</p> <p>CO4: Analyse user defined primitives in Verilog HDL.</p> <p>CO5: Apply the knowledge of different types of digital modelling in Verilog HDL.</p> <p>CO6: Justify the implementation of Verilog code of several digital circuits using Verilog HDL and their test benches.</p>
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10. Details of the Course

S. No.	Contents	Contact Hours
1.	<p>Unit 1: Basic Concepts: Lexical conventions, Data types, System tasks and compiler directives.</p> <p>Modules and Ports: Modules, Ports, Hierarchical names.</p> <p>Gate-Level Modeling: Gate types, Gate delays.</p>	8
2.	<p>Unit 2: Dataflow Modelling: Continuous assignments, Delays, Expressions, Operators and Operands. Operator types, Examples.</p> <p>Behavioural Modelling: Structured procedures, Procedural assignments, Timing controls, Conditional statements, Multiway branching, Loops, Sequential and parallel Blocks, Generate blocks, Examples.</p>	10
3.	Unit 3: Task and Functions:	10

	<p><i>Differences between tasks and functions, Tasks, Functions.</i></p> <p>Useful Modelling Techniques:</p> <p><i>Procedural continuous assignments, Overriding parameters, Conditional compilation and execution, Time scales, Useful system tasks.</i></p> <p>Timing and Delays:</p> <p><i>Types of delay models, Path delay modelling, Timing checks, Delay back-annotation.</i></p>	
4.	<p>Unit 4: Switch-Level Modelling:</p> <p><i>Switch-Modelling elements, examples.</i></p> <p>User-Defined Primitives:</p> <p><i>UDP basics, Combinational UDPs, Sequential UDPs, UDP table shorthand symbols, Guidelines for UDP design.</i></p>	10
5.	<p>Unit 5: Writing Test Benches:</p> <p><i>Basic test benches, Test bench structure, Constrained random stimulus generation, Object-oriented programming and Assertion-based verification.</i></p>	7
	Total	45

11. Suggested Books

S. No.	Name of Authors/Books/Publishers	Edition	Year of Publication / Reprint
	Textbooks		
1.	Samir Palnitkar, “ Verilog HDL ”, Pearson Education	2 nd	2003
2.	Mark Zwolinski, “ Digital System Design with System Verilog ”, Pearson Education	1 st	2009
	Reference Books		
1.	J. Bhasker, “ Verilog HDL Synthesis-A practical Primer ”, Star galaxy Press	1 st	1998
2.	J. Bhasker, “ Verilog HDL Primer ”, Pearson Education.	3 rd	2015

12.	Mode of Evaluation	Test / Quiz / Assignment / Mid Term Exam / End Term Exam
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GRAPHIC ERA (DEEMED TO BE UNIVERSITY), DEHRADUN

SEMESTER II

S. No.	Department of Electronics and Communication Engineering						
1.	Subject Code	VDM 203	Course Title		Advanced VLSI Circuit Testing		
2.	Contact Hours	L	3	T	0	P	0
3.	Examination Duration	Theory		3	Practical		0
4.	Relative Weight	CIE	25	MSE	25	ESE	50
5.	Credit	03					
6.	Semester	Second					
7.	Category of Course	DSC/PCC					
8.	Pre-requisite	VLSI Technology					

9.	Course Outcomes	<p>After completion of the course the students will be able to:</p> <p>CO1: Recall the knowledge of fault modeling and fault simulation.</p> <p>CO2: Understand ATPG algorithm for combinational and sequential circuits</p> <p>CO3: Apply the knowledge of high-level testability Measures, SCOAP controllability and observability.</p> <p>CO4: Analyze different memory testing algorithms</p> <p>CO5: Assess and evaluate scan architecture</p> <p>CO6: Design testing algorithms for VLSI components</p>
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10. Details of the Course

S. No.	Contents	Contact Hours
1.	<p>Unit 1: Introduction: Role of testing, Digital and analog VLSI testing, VLSI technology trends affecting testing.</p> <p>VLSI Testing Process and Test Equipment: Types of testing, Automatic test equipment, Multi-Site testing, Electrical parametric testing.</p> <p>Test Economics and Product Quality: Defining costs, Production benefit-cost analysis, Economics of testable design, The rule of ten, Yield, Test data analysis.</p> <p>Fault Modelling: Defects, Errors and Faults, Functional versus Structural testing, A glossary of fault models, Single stuck-at fault,</p> <p>Logic and Fault Simulation: Simulation for design verification, Simulation for test evaluation.</p>	12
2.	<p>Unit 2: Testability Measures: SCOAP controllability and observability, High-level testability measures.</p>	10

	Combinational Circuit Test Generation: <i>Algorithms and representations, Redundancy identification (RID), Testing as a global problem, Definitions, Test generation systems, Test compaction, Significant combinational ATPG algorithms and sequential circuit test generation.</i>	
3.	Unit 3: Memory Test: <i>Memory density and defect trends, Faults, Memory test levels, March test notation, Fault modelling, Memory testing. Analog and mixed signal test, Delay test and IDDQ test.</i>	7
4.	Unit 4: Fundamental Techniques for Logic Testing: <i>DFT fundamentals, ATPQ fundamental, Scan architecture and technique.</i>	7
5.	Unit 5: Embedded Core Test Fundamentals: <i>Introduction to embedded core testing, Core, Core-based design, Reuse core deliverables, Core DFT issues, Development of reusable core, Scan testing the isolated core, Scan testing the non-core logic, User defined logic chip-level DFT concerns, Memory testing with BIST.</i>	9
	Total	45

11. Suggested Books

S. No.	Name of Authors/Books/Publishers	Edition	Year of Publication / Reprint
	Textbooks		
1.	Viswani D. Agarwal, Michael L. Bushnell, “ Essentials of electronic testing for digital memory & mixed signal VLSI circuit ”, Kluwer Academic Publications	1 st	1999
2.	Alfred L. Crouch, “ Design for test for digital IC's and embedded core systems ”, PHI	1 st	1999
	Reference Books		
1.	Parag. K. Lala, “ Digital circuit testing and testability ”, Academic Press	1 st	1997
2.	Ashok K. Sharma, “ Semiconductor memories technology, testing and reliability ”, Prentice-Hall of India Private Limited, New Delhi	1 st	1997

12.	Mode of Evaluation	Test / Quiz / Assignment / Mid Term Exam / End Term Exam
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GRAPHIC ERA (DEEMED TO BE UNIVERSITY), DEHRADUN

SEMESTER II

S. No.	Department of Electronics and Communication Engineering						
1.	Subject Code	VDM 204	Course Title		Low Power VLSI Design		
2.	Contact Hours	L	3	T	0	P	0
3.	Examination Duration	Theory		3	Practical		0
4.	Relative Weight	CIE	25	MSE	25	ESE	50
5.	Credit	03					
6.	Semester	Second					
7.	Category of Course	DSC/PCC					
8.	Pre-requisite	Advanced Digital Integrated Circuit					

9.	Course Outcomes	<p>After completion of the course the students will be able to:</p> <p>CO1: Acquire the fundamental knowledge of low power VLSI design,</p> <p>CO2: Infer about static and dynamic power dissipation.</p> <p>CO3: Ability to implement logic circuits and advanced low power design techniques.</p> <p>CO4: Analyse different techniques required to minimize the leakage power.</p> <p>CO5: Evaluate the characteristics low power analog and digital circuits.</p> <p>CO6: Design of low power memory devices.</p>
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10. Details of the Course

S. No.	Contents	Contact Hours
1.	Unit 1: Introduction to Low Power VLSI: Overview, Need for Low Power VLSI Digital Integrated Circuits, Basic Principles of Low Power Design, Physics of Power Dissipation; Technology and Device Effect on Low Power: Transistor Sizing, Gate Oxide Thickness, Impact of Technology Scaling, Technology & Device innovation.	10
2.	Unit 2: Sources of Power Dissipation in MOS Devices: Power Estimation, Dynamic Power Dissipation: Short Circuit Power, Switching Power, Glitching Power; Static Power Dissipation, Probabilistic Power Analysis, Degrees of Freedom.	10
3.	Unit 3: Logic Circuits and Advanced Techniques: Logic circuits, Special Techniques: Architecture and Systems; Emerging Low power Techniques, Physics of Power Dissipation in CMOS FET Devices; Design of Low Power CMOS Circuits, Supply Voltage Scaling Approaches; Switched Capacitance minimization Approaches.	9

4.	Unit 4: Leakage Power Minimization Approaches: <i>Synthesis in Low Power Design, Test of Low Voltages CMOS Circuits; Variable threshold Voltage CMOS (VTCMOS) Approach, Multi threshold Voltage CMOS (MTCMOS) approach, Power gating Transistor Stacking, Dual- threshold Voltage (V_t) Assignment Approach (DTCMOS).</i>	8
5.	Unit 5: Low Power Techniques: <i>Low Power Static RAM Architectures, Low Power SRAM/DRAM Design, Low Energy Computing using Energy Recovery Techniques, Software Design for Low Power, CAD Tools for Low Power Synthesis.</i>	8
	Total	45

II. Suggested Books

S. No.	Name of Authors/Books/Publishers	Edition	Year of Publication / Reprint
	Textbooks		
1.	Gary Yeap, " Practical Low Power Digital VLSI Design ", Springer.	1 st	1998
2.	Kaushik Roy and Sharat Prasad, " Low Power CMOS VLSI Circuit Design " Wiley.	1 st	2000
	Reference Books		
1.	J. B. Kuo and J. H. Lou, Low " Voltage CMOS VLSI Circuits ", Wiley.	1 st	1999
2.	J. M. Rabaey, A. P. Chandrakasan and B. Nikolic, " Digital Integrated Circuits: A Design Perspective ", Pearson	2 nd	2003

12.	Mode of Evaluation	Test / Quiz / Assignment / Mid Term Exam / End Term Exam
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GRAPHIC ERA (DEEMED TO BE UNIVERSITY), DEHRADUN

SEMESTER II

S. No.	Department of Electronics and Communication Engineering						
1.	Subject Code	VDM 251	Course Title		Verilog HDL Lab		
2.	Contact Hours	L	0	T	0	P	4
3.	Examination Duration	Theory		0	Practical		4
4.	Relative Weight	CIE	25	MSE	25	ESE	50
5.	Credit	02					
6.	Semester	Second					
7.	Category of Course	DSC/LC					
8.	Pre-requisite	Digital Electronics					

9.	Course Outcomes	<p>After completion of the course the students will be able to:</p> <p>CO1: Understand digital circuit designing through Verilog HDL.</p> <p>CO2: Implement digital logic circuits using Verilog HDL.</p> <p>CO3: Analyse various combinational and sequential circuits using Verilog HDL simulation.</p> <p>CO4: Design various digital systems using Verilog HDL.</p>
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10. Details of the Course

S. No.	List of problems for which student should develop program and execute in the Laboratory	Contact Hours
1.	Design and simulation of Half Adder, Half Subtractor, Full Adder and Full Subtractor Circuit Using all modelling styles.	2
2.	Design and simulation of n-bit comparator using behavioural modelling and parameter statement.	2
3.	Design and simulation of 8-bit Adder/Subtractor Circuit using Structural modelling and generic Statement.	2
4.	Design and simulation of 4-bit ALU using behavioural modelling.	2
5.	Design and simulation of 4-bit Carry-Look ahead Adder.	2
6.	Design and simulation of Flip-flops and Latches (JK, D, T, SR).	2
7.	Design and simulation of MOD-n UP/DOWN Counter.	2
8.	Design and simulation of n-bit Universal Shift Register.	2
9.	Design and simulation of 4-bit Binary Multiplier and 4-bit Tree Multiplier.	2
10.	Design and simulation of Booths Algorithm for signed multiplication.	2
11.	Design and simulation of 32-bit floating-point multiplier.	2
12.	Design and simulation of 32-bit floating-point adder.	2
13.	Design and simulation of Traffic Light Controller using FSM.	2
14.	FPGA Implementation of Ring and Johnson Counter.	2
	Total	28



<i>Innovative Experiments</i>		
13.	<i>FPGA Implementation of Flip-flops timing and power analysis.</i>	2
14.	<i>Design and simulation of binary division..</i>	2
15.	<i>Design and simulation of floating-point divider.</i>	2
16.	<i>As suggested by faculty and lab in-charge.</i>	2
	Total	08

11. Suggested Books

<i>S. No.</i>	<i>Name of Authors/Books/Publishers</i>	<i>Edition</i>	<i>Year of Publication / Reprint</i>
	Textbooks		
1.	Samir Palnitkar, “ Verilog HDL ”, Pearson Education	2 nd	2003
2.	Mark Zwolinski, “ Digital System Design with System Verilog ”, Pearson Education	1 st	2009
	Reference Books		
1.	J. Bhasker, “ Verilog HDL Synthesis-A practical Primer ”, Star galaxy Press	1 st	1998
2.	J. Bhasker, “ Verilog HDL Primer ”, Pearson Education.	3 rd	2015

12..	Mode of Evaluation	Test / Quiz / Assignment / Mid Term Exam / End Term Exam
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GRAPHIC ERA (DEEMED TO BE UNIVERSITY), DEHRADUN

SEMESTER II

S. No.	Department of Electronics and Communication Engineering						
1.	Subject Code	VDM 252	Course Title		VLSI Physical Design Lab		
2.	Contact Hours	L	0	T	0	P	4
3.	Examination Duration	Theory		0	Practical		4
4.	Relative Weight	CIE	25	MSE	25	ESE	50
5.	Credit	02					
6.	Semester	Second					
7.	Category of Course	DSC/LC					
8.	Pre-requisite	Digital Electronics, Advanced Digital Integrated Circuit					

9.	Course Outcomes	<p>After completion of the course the students will be able to:</p> <p>CO1: Understand Linux environment, tools, and basic scripting.</p> <p>CO2: Apply the concepts of physical design for VLSI chip.</p> <p>CO3: Analyse placement, routing, and power Planning for different circuits.</p> <p>CO4: Design circuits using Verilog HDL, waveform Debugging, and synthesis</p>
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10. Details of the Course

S. No.	List of problems for which student should develop program and execute in the Laboratory	Contact Hours
1.	Familiarization with Linux environment, and basic scripting Verilog HDL in cadence Tool.	2
2.	Design, simulation, and test of an 8-bit counter with instructions Verilog HDL in cadence Tool.	2
3.	Synthesis of 8-bit counter circuit with instructions Verilog HDL in cadence Tool.	2
4.	Placement and power planning of 8-bit counter circuit in cadence digital implementation tool of 8-bit counter circuit.	2
5.	Routing of 8-bit counter circuit in cadence digital implementation tool in gpdn 90 technology.	2
6.	Design, simulation, and test of a parallel adder with instructions Verilog HDL in cadence Tool.	2
7.	Synthesis of Parallel adder circuit with instructions Verilog HDL in cadence Tool.	2
8.	Placement and power planning of Parallel adder circuit in Cadence digital implementation tool of Parallel adder circuit.	2
9.	Routing of Parallel adder circuit in Cadence digital implementation tool in gpdn 90 nm technology.	2

10.	Design, simulation, and test of a Booth's Multiplier with instructions Verilog HDL in cadence Tool.	2
11.	Design, simulation, and test of a Universal Shift Register with instructions Verilog HDL in cadence Tool.	2
12.	Synthesis of Universal Shift Register with instructions Verilog HDL in cadence Tool.	2
	Total	24
Innovative Experiments		
13.	Design, simulation, and test of a ALU circuit with instructions Verilog HDL in cadence Tool.	2
14.	Routing of ALU Circuit in Cadence Digital Implementation tool in gpdk 90 nm technology.	2
15.	Design, simulation, and Test of a SRAM with instructions Verilog HDL in cadence Tool.	2
	Total	06

11. Suggested Books

S. No.	Name of Authors/Books/Publishers	Edition	Year of Publication / Reprint
	Textbooks		
1.	Samir Palnitkar, "Verilog HDL", Pearson Education	2 nd	2003
2.	J. M. Rabaey, A. P. Chandrakasan and B. Nikolic, "Digital Integrated Circuits: A Design Perspective", Pearson	2 nd	2003
	Reference Books		
1.	J. Bhasker, "Verilog HDL Synthesis-A practical Primer", Star galaxy Press	1 st	1998
2.	J. Bhasker, "Verilog HDL Primer", Pearson Education.	3 rd	2015

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GRAPHIC ERA (DEEMED TO BE UNIVERSITY), DEHRADUN

SEMESTER III

S. No.	Department of Electronics and Communication Engineering						
1.	Subject Code	VDM 301	Course Title		VLSI Physical Design Automation		
2.	Contact Hours	L	3	T	0	P	0
3.	Examination Duration	Theory		3	Practical		0
4.	Relative Weight	CIE	25	MSE	25	ESE	50
5.	Credit	03					
6.	Semester	Third					
7.	Category of Course	DSC/PCC					
8.	Pre-requisite	Basic Electronics Engineering, Digital Electronics.					

9.	Course Outcomes	<p>After completion of the course the students will be able to:</p> <p>CO1: Recall the concepts of VLSI design automation tools.</p> <p>CO2: Understand different layout compaction, placement, and routing algorithms.</p> <p>CO3: Apply the concepts of Logic Synthesis in VLSI design.</p> <p>CO4: Analyze floor planning and routing algorithms.</p> <p>CO5: Assess and evaluate scheduling algorithms, allocation, and assignment.</p> <p>CO6: Optimize design layouts for floor-planning, placement, and routing..</p>
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10. Details of the Course

S. No.	Contents	Contact Hours
1.	Unit 1: VLSI Design Automation Tools: Design cycle, Design styles, Algorithms and system design, Structural and logic design, Transistor level design, Layout design, Verification methods, Design management tools.	10
2.	Unit 2: Layout Compaction, Placement and Routing: Design rules, Symbolic layout, Applications of compaction, Formulation methods, Algorithms for constrained graph compaction, Circuit representation, Wire length estimation, Placement algorithms, Partitioning algorithms.	10
3.	Unit 3: Floor Planning and Routing: Floor planning concepts, Shape functions and Floor planning, Sizing, Local routing, Area routing, Channel routing, Global routing and its algorithms.	8
4.	Unit 4: Simulation and Logic Synthesis:	9



	Gate level and switch level modelling and simulation. Introduction to combinational logic synthesis, ROBDD principles, Implementation, Construction and manipulation, Logic synthesis.	
5.	Unit 5: High-Level Synthesis: Hardware model for high level synthesis, Internal representation of input algorithms, Allocation, Assignment and scheduling, Scheduling algorithms. Aspects of assignment.	8
	Total	45

11. Suggested Books

S. No.	Name of Authors/Books/Publishers	Edition	Year of Publication / Reprint
	Textbooks		
1.	S. H. Gerez, “ <i>Algorithms for VLSI Design Automation</i> ”, John Wiley.	3 rd	2000
2.	N. A. Sherwani, “ <i>Algorithms for VLSI Physical Design Automation</i> ”, Kluwer.	3 rd	1999
	Reference Books		
1.	M. Sait, H. Youssef, “ <i>VLSI Physical Design Automation</i> ”, World scientific.	1 st	1999
2.	M. Sarrafzadeh, “ <i>Introduction to VLSI Physical Design</i> ”, McGraw Hill (IE).	1 st	1996

12.	Mode of Evaluation	Test / Quiz / Assignment / Mid Term Exam / End Term Exam
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GRAPHIC ERA (DEEMED TO BE UNIVERSITY), DEHRADUN

SEMESTER III

Sr. No.	Department of Electronics and Communication Engineering						
1.	Subject Code	VDM 302	Course Title		Research Methodology and IPR		
2.	Contact Hours	L	02	T	0	P	0
3.	Examination Duration	Theory		03	Practical		0
4.	Relative Weight	CIE	25	MSE	25	ESE	50
6.	Credit	02					
6.	Semester	Third					
7.	Category of Course	SEC/ESC					
8.	Pre-requisite	Basic Knowledge of Research					

9.	Course Outcomes	<p>After completion of the course the students will be able to:</p> <p>CO1: Understand research problem formulation.</p> <p>CO2: Analyze research related information and Follow research ethics in technical writing.</p> <p>CO3: Understand the concept and importance of IPR and scope of patent rights.</p> <p>CO4: Understand that today's world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity.</p>
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10. Details of the Course

Sl. No.	Contents	Contact Hours
1.	<p>Unit 1: RESEARCH METHODOLOGY</p> <p>Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, Plagiarism, Research ethics.</p>	06
2.	<p>Unit 2: RESULTS, ANALYSIS & TECHNICAL WRITING</p> <p>Importance and scientific methodology in recording results, importance of negative results, different ways of recording, industrial requirement, artifacts versus true results, types of analysis (analytical, objective, subjective), outcome as new idea, hypothesis, concept, theory, model etc. Effective technical writing, how to write a manuscript/ responses to reviewers comments, preparation of research article/ research report,</p>	12

	<i>Writing a Research Proposal - presentation and assessment by a review committee.</i>	
3.	Unit 3: INTELLECTUAL PROPERTY RIGHTS & PATENT RIGHTS <i>Nature of Intellectual Property: Patents, Designs, Trade Mark and Copyright. Process of Patenting and Development: technological research, innovation, patenting & development. Procedure for grants of patents, Patenting under PCT.</i> <i>Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications. New Developments in IPR: Administration of Patent System.</i>	12
	Total	30

11. Suggested Books

SL. No.	Name of Authors/Books/Publishers	Edition	Year of Publication / Reprint
	Textbooks		
1.	Ranjit Kumar, “ Research Methodology- A step by step guide for beginners ”, Pearson Education.	2 nd	2005
2.	Ann M. Korner, “ Guide to Publishing a Scientific paper ”, Bioscript Press.	2 nd	2004
3.	T. Ramappa, “ Intellectual Property Rights Under WTO ”, S. Chand.	2 nd	2008
	Reference Books		
1.	Debora J. Halbert, “ Resisting Intellectual Property ”, Taylor & Francis Ltd .	1 st	2007
2.	Robert P. Merges, Peter S. Menell, Mark A. Lemley, “ Property in New Technological Intellectual Age ”, Aspen Law & Business;.	3 rd	2016
3.	T. Ramappa, “ Intellectual Property Rights Under WTO ”, S. Chand, Wheeler Publications.	2 nd	2008

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GRAPHIC ERA (DEEMED TO BE UNIVERSITY), DEHRADUN

SEMESTER III

S. No.	Department of Electronics and Communication Engineering						
1.	Subject Code	VDM 351	Course Title		Modelling and Simulation Lab		
2.	Contact Hours	L	0	T	0	P	4
3.	Examination Duration	Theory		0	Practical		4
4.	Relative Weight	CIE	25	MSE	25	ESE	50
5.	Credit	02					
6.	Semester	Third					
7.	Category of Course	DSC/LC					
8.	Pre-requisite	Digital Electronics, Advanced Digital Integrated Circuit					

9.	Course Outcomes	<p>After completion of the course the students will be able to:</p> <p>CO1: Understand various semiconductor devices and circuit using simulators</p> <p>CO2: Compute the characteristics of various digital and analog systems.</p> <p>CO3: Analyze Cadence, VTCAD and Xilinx tools for the implementation of digital and analog circuits</p> <p>CO4: Evaluate various MOS devices performance using MATLAB and VTCAD</p>
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10. Details of the Course

S. No.	List of problems for which student should develop program and execute in the Laboratory	Contact Hours
1.	Study of Cadence tool for the implementation of Multistage Amplifier.	2
2.	Study of Cadence tool for the implementation of analog circuits (CS Amplifier).	2
3.	Implementation of a novel circuit and its performance analysis using Cadence tool (Flip-Flops using pass transistors).	2
4.	Design and simulation of CMOS (NMOS/PMOS) using VTCAD and their characteristics analysis.	2
5.	Design and simulation of Dual Gate MOSFET using VTCAD and their characteristics analysis.	2
6.	Design and simulation of Gate All Around FET (GAA-FET) using VTCAD and their characteristics analysis.	2
7.	Design and simulation of BJT using VTCAD and their characteristics analysis.	2
8.	Study of OrCAD tool for analysis of RC coupled amplifier.	2

9.	To plot the drain characteristics for n-channel MOSFET using MATLAB for implementation of MOSFET models in linear and saturation region.	2
10.	To plot the transfer characteristics for n-channel MOSFET in linear region and extract the various parameters (like threshold voltage (V_{th}), Transconductance (g_m), Mobility (μ) and on-off current ratio (I_{on}/I_{off}) using MATLAB.	2
11.	To plot the transfer characteristics for n-channel MOSFET in saturation region and extract the various parameters (like threshold voltage (V_{th}), Transconductance (g_m), Mobility(μ) and on-off current ratio (I_{on}/I_{off}) using MATLAB.	2
12.	Write a program for the following condition using Xilinx. Government wants to give subsidy to the citizens, so they decided that if income is greater than subsidy then income itself is the final income. Otherwise, subsidy will be added to income to get the total income.	2
Total		24
Innovative Experiments		
13.	FPGA implementation of various logic gates in Xilinx tool.	2
14.	Design and Simulation of universal gates in VTCAD tool.	2
15.	Design and Simulation of Tri-Gate in VTCAD tool.	2
Total		06

11. Suggested Books

S. No.	Name of Authors/Books/Publishers	Edition	Year of Publication / Reprint
Textbooks			
1.	R. Jacob Baker, H. W. Li, and D.E. Boyce, “ CMOS circuit design, Layout and simulation ”, Prentice-Hall of India.	1 st	1998
2.	J. M. Rabaey, A. P. Chandrakasan and B. Nikolic, “ Digital Integrated Circuits: A Design Perspective ”, Pearson	2 nd	2003
Reference Books			
1.	S. Kang and Y. Leblebici, “ CMOS Digital Integrated Circuits, Analysis and Design ”, Tata McGraw-Hill.	3 rd	2003

12.	Mode of Evaluation	Test / Quiz / Assignment / Mid Term Exam / End Term Exam
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GRAPHIC ERA (DEEMED TO BE UNIVERSITY), DEHRADUN

SEMESTER I

S. No.	Department of Electronics and Communication Engineering						
1.	Subject Code	VDM 141	Course Title		Advanced Nanotechnology		
2.	Contact Hours	L	3	T	0	P	0
3.	Examination Duration	Theory		3	Practical		0
4.	Relative Weight	CIE	25	MSE	25	ESE	50
5.	Credit	03					
6.	Semester	First					
7.	Category of Course	DSE/PEC					
8.	Pre-requisite	Physics, Chemistry					

9.	Course Outcomes	<p>After completion of the course the students will be able to:</p> <p>CO1: Remember the concepts of emerging world of nanoscience, Knowledge of single-electron devices and carbon based nanoelectronics devices.</p> <p>CO2: Understand the various top-down and bottom-up approaches for nanomaterial synthesis.</p> <p>CO3: Apply the acquired knowledge to develop novel nanomaterials.</p> <p>CO4: Analyze the properties of nanomaterials using various scanning probe techniques and spectroscopic techniques for material characterization.</p> <p>CO5: Evaluate the performance of nanotechnology related devices for various industrial applications.</p> <p>CO6: Utilize analytical tools in nanoscale engineering.</p>
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10. Details of the Course

S. No.	Contents	Contact Hours
1.	Unit 1: Introduction to Nanotechnology: Overview, Historical background, Importance of nanoscale, Bottom-up approaches, Top-down approaches, Functional approaches.	8
2.	Unit 2: Nano Materials: Fundamental concepts of nanomaterials, Allotropes of carbon, Graphene, Graphene nanoribbons, Fullerenes, Fullerites, Carbon nanotubes (CNTs), Bucky paper.	8
3.	Unit 3: Nano Electronics: Approaches to Nano electronics, Fabrication of integrated circuits, Introduction to microelectromechanical systems (MEMS), Nanoelectromechanical systems (NEMS), Nanowires, Nano-Circuits, Quantum wire, Quantum well.	10

4.	Unit 4: Nano-Engineering Devices and Nano- Medicine: <i>Lab on chip, Micromachinery, Nanomotor, Nanopore, Nano sensor, Quantum point contact, Synthetic molecular motors, Medical applications of nanomaterials.</i>	9
5.	Unit 5: Analytical Tools in Nanoscale Engineering and Nanolithography: <i>Atomic force microscopy (AFM), Scanning tunnelling microscope (STM), Nanolithography: Dip-pen, Electron beam, Ion-beam sculpting, Nanoimprint lithograph, Photolithography.</i>	10
Total		45

11. Suggested Books

S. No.	Name of Authors/Books/Publishers	Edition	Year of Publication / Reprint
Textbooks			
1.	Shunri Oda, David Ferry, “ Nanoscale Silicon Devices ”, CRC Press, Taylor & Francis Group.	1 st	2016
2.	Robert Puer, “ Nanoelectronics: Materials, Devices, Applications ”, Wiley.	1 st	2017
Reference Books			
1.	Suprio Datta, “ Lessons from nanoelectronics ”, World Scientific publisher.	1 st	2012
2.	Gabriel M. Rebeiz, “ RF MEMS: Theory, Design, and Technology ”, Wiley.	1 st	2003
3.	Julian W. Gardner, “ Microsensors, MEMS and Smart Devices ”, Wiley.	1 st	2002

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GRAPHIC ERA (DEEMED TO BE UNIVERSITY), DEHRADUN

SEMESTER I

S. No.	Department of Electronics and Communication Engineering						
1.	Subject Code	VDM 142	Course Title		Optimization Techniques in VLSI Design		
2.	Contact Hours	L	3	T	0	P	0
3.	Examination Duration	Theory		3	Practical		0
4.	Relative Weight	CIE	25	MSE	25	ESE	50
5.	Credit	03					
6.	Semester	First					
7.	Category of Course	DSE/PEC					
8.	Pre-requisite	VLSI Technology and Design					

9.	Course Outcomes	<p>After completion of the course the students will be able to:</p> <p>CO1: Recall the knowledge of modelling techniques based on incorporating empirical parameters.</p> <p>CO2: Understand the performance parameters and yield estimation of optimization techniques.</p> <p>CO3: Apply the knowledge of convex optimization techniques.</p> <p>CO4: Analyse and understand Genetic algorithm in VLSI design.</p> <p>CO5: Assess and evaluate FPGA for automatic test generation.</p> <p>CO6: Implement optimization techniques in VLSI design.</p>
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10. Details of the Course

S. No.	Contents	Contact Hours
1.	Unit 1: Statistical Modelling: Modelling sources of variations, Monte Carlo techniques, Process variation modelling- Pelgrom's model, Principal component-based modelling, Quad tree based modelling, Performance modelling-response Surface methodology, Delay modelling, Interconnect delay models.	9
2.	Unit 2: Statistical Performance, Power and Yield Analysis: Statistical timing analysis, Parameter space techniques, Bayesian networks leakage models, High level statistical analysis, Gate level statistical analysis, Dynamic power, Leakage power, Temperature and power supply variations, High level yield estimation and Gate level yield estimation.	9
3.	Unit 3: Convex Optimization: Convex sets, Convex functions, Geometric programming, Trade-off and sensitivity analysis, Generalized geometric programming, Geometric programming applied to digital circuit gate sizing, Floor planning, Wire sizing, Approximation and fitting- monomial fitting, Maxmonomial fitting, Posynomial fitting.	10

4.	Unit 4: Genetic Algorithm: Introduction, GA Technology-Steady state algorithm-Fitness scaling-Inversion GA for VLSI design, Layout and test automation- Partitioning-automatic placement, Routing technology, Mapping for FPGA- Automatic test generation- Partitioning algorithm taxonomy-multiway partitioning Hybrid Genetic-Encoding-Local Improvement-WDFR comparison of cas-standard cell placement-GASP algorithm-unified algorithm.	9
5.	Unit 5: GA Routing Procedures and Power Estimation: Global routing-FPGA technology mapping-circuit Generation-Test Generation in A GA framework-test generation procedure. Power estimation-application of GA-standard cell placement-GA for ATG-problem encoding- fitness function-GA Vs conventional algorithm. Hardware/Software Co-Designs.	8
	Total	45

11. Suggested Books

S. No.	Name of Authors/Books/Publishers	Edition	Year of Publication / Reprint
	Textbooks		
1.	Ashish Srivastava, Dennis Sylvester, David Blaauwi, "Statistical Analysis and Optimization for VLSI: Timing and Power", Springer.	1 st	2005
2.	Kalyanmoy Dev, "Optimization for Engineering Design: Algorithms and Examples", PHI Learning.	2 nd	2001
	Reference Books		
1.	Pinaki Mazumder, E. Mrudnick, "Genetic Algorithm for VLSI Design, Layout and test Automation", Prentice Hall.	1 st	2002

12.	Mode of Evaluation	Test / Quiz / Assignment / Mid Term Exam / End Term Exam
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GRAPHIC ERA (DEEMED TO BE UNIVERSITY), DEHRADUN

SEMESTER I

S. No.	Department of Electronics and Communication Engineering						
1.	Subject Code	VDM 143	Course Title		Theory and Application of Embedded Systems		
2.	Contact Hours	L	3	T	0	P	0
3.	Examination Duration	Theory		3	Practical		0
4.	Relative Weight	CIE	25	MSE	25	ESE	50
5.	Credit	03					
6.	Semester	First					
7.	Category of Course	DSE/PEC					
8.	Pre-requisite	Microcontrollers & Embedded Systems					

9.	Course Outcomes	<p>After completion of the course the students will be able to:</p> <p>CO1: Recall the basic concept of embedded system.</p> <p>CO2: Understand the architecture and instruction sets of PIC microcontrollers.</p> <p>CO3: Relate the knowledge of system firmware design.</p> <p>CO4: Analyse structure of RTOS based embedded systems.</p> <p>CO5: Evaluate ARM-32 bit processors as the advanced series microcontroller.</p> <p>CO6: Integrate the concepts of advanced embedded systems for developing projects.</p>
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10. Details of the Course

S. No.	Contents	Contact Hours
1.	Unit 1: Embedded Systems: Embedded vs General computing system, classification, application and purpose of Embedded system. Core of an Embedded System, Memory, Sensors, Actuators. Characteristics and quality attributes of embedded systems.	9
2.	Unit 2: PIC Architectures: PIC series of microcontrollers, Assembly basics, Instruction list and description, Addressing modes, Interrupts and timer.	8
3.	Unit 3: System Firmware Design: Hardware Software Co-Design, embedded firmware design approaches, computational models, embedded firmware development languages, Integration and testing of Embedded Hardware and firmware.	9



4.	Unit 4: RTOS Based Embedded System Design: Basics of Operating systems, Types of Operating Systems, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling.	9
5.	Unit 5: ARM-32 bit Microcontroller: Thumb-2 technology and applications of ARM, Architecture of ARM Cortex M3, Various Units in the architecture, General Purpose Registers, Special Registers, exceptions, interrupts, stack operation.	10
	Total	45

11. Suggested Books

S. No.	Name of Authors/Books/Publishers	Edition	Year of Publication / Reprint
	Textbooks		
1.	Raj Kamal, “Microcontrollers: Architecture, Programming, Interfacing and System Design”, Pearson Education India.	2 nd	2005
2.	J. Morton, “The PIC Microcontroller”, Newnes.	3 rd	2005
	Reference Books		
1.	A. Sloss, D. Symes, C. Wright, “ARM System Developer’s Guide: Designing and optimizing system software”, Morgan Kauffman Publisher.	1 st	2004
2.	K. V. Shibhu, “Introduction to Embedded Systems”, Tata McGraw Hill.	1 st	2009
3.	Frank Vahid, Tony Givargis, “Embedded System Design, A Unified Hardware, Software Approach”, Wiley Publications.	3 rd	1999

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GRAPHIC ERA (DEEMED TO BE UNIVERSITY), DEHRADUN

SEMESTER I

S. No.	Department of Electronics and Communication Engineering						
1.	Subject Code	VDM 144	Course Title		Digital Signal Processing for VLSI		
2.	Contact Hours	L	3	T	0	P	0
3.	Examination Duration	Theory		3	Practical		0
4.	Relative Weight	CIE	25	MSE	25	ESE	50
5.	Credit	03					
6.	Semester	First					
7.	Category of Course	DSE/PEC					
8.	Pre-requisite	Digital Signal Processing					

9.	Course Outcomes	<p>After completion of the course the students will be able to:</p> <p>CO1: Recall the basic concepts of DSP Algorithms.</p> <p>CO2: Understand iteration bound, pipelining and parallel processing.</p> <p>CO3: Apply the knowledge of retiming and parallel processing by using various fast convolution techniques.</p> <p>CO4: Analyse algorithmic strength reduction in filters transforms and pipelined and parallel recursive filters.</p> <p>CO5: Evaluate scaling and round off noise computation processes.</p> <p>CO6: Design and develop low power VLSI based DSP architecture.</p>
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10. Details of the Course

S. No.	Contents	Contact Hours
1.	<p>Unit 1:</p> <p>Introduction to DSP Systems: Introduction to VLSI DSP, Typical DSP Algorithms, DSP Application demands, Scaled CMOS technologies, Representation of DSP algorithms.</p> <p>Iteration Bound: Data-Flow graph representations, Loop bound and Iteration bound, Algorithms for computing Iteration Bound.</p>	8
2.	<p>Unit 2:</p> <p>Pipelining and Parallel Processing: Pipelining of FIR digital filters, Parallel Processing, Pipelining and Parallel Processing for Low power.</p> <p>Retiming, Unfolding and Folding: Definitions and Properties of Retiming, Solving systems of Inequalities, Retiming Techniques, Algorithm for Unfolding, Properties, Critical Path, Unfolding and retiming, Folding transformation, Register minimization techniques, Register minimization in folded architectures, folding of multi-rate systems.</p>	10

3.	Unit 3: Systolic Architecture Design: Introduction, Systolic Array Design Methodology, FIR Systolic Arrays, Selection of scheduling Vector. Scaling and Roundoff noise, State Variable description of digital filters, Noise computation Fast Convolution: Introduction, Cook-Toom algorithm, Winograd algorithm, Iterated Convolution, Cyclic Convolution.	10
4.	Unit 4: Bit-Level Arithmetic Architecture: Parallel Multipliers, Interleaved floor-plan and Bit-Plane based digital filters, Bit-serial Multipliers, Bit-Serial Filter Design and Implementation, Canonic Signed Digit Arithmetic. Redundant Arithmetic: Redundant Number System, Carry-free Radix-2 Addition and Subtraction, Hybrid Radix-4 Addition, Radix-2 Hybrid Redundant Multiplication Architectures.	8
5.	Unit 5: Low Power Design: Scaling versus power consumption, Power Analysis, Power Reduction Techniques, Power Estimation Approaches. Programmable Digital Signal Processors: Evolution and features of Programmable Digital Signal Processors, DSP processors for Mobile and Wireless Communications, Processors for Multimedia Signal Processing.	9
Total		45

11. Suggested Books

S. No.	Name of Authors/Books/Publishers	Edition	Year of Publication / Reprint
	Textbooks		
1.	K. K. Parhi, "VLSI Digital Signal Processing", John-Wiley	1 st	1999
2.	John G. Proakis, Dimitris G. Manolakis, "Digital Signal Processing", Prentice Hall of India.	3 rd	1996
	Reference Books		
1.	Richard J. Higgins, "Digital signal processing in VLSI", Prentice Hall.	1 st	1990

12.	Mode of Evaluation	Test / Quiz / Assignment / Mid Term Exam / End Term Exam
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GRAPHIC ERA (DEEMED TO BE UNIVERSITY), DEHRADUN

SEMESTER II

S. No.	Department of Electronics and Communication Engineering						
1.	Subject Code	VDM 241	Course Title		Micro-Sensors and MEMS		
2.	Contact Hours	L	3	T	0	P	0
3.	Examination Duration	Theory		3	Practical		0
4.	Relative Weight	CIE	25	MSE	25	ESE	50
5.	Credit	03					
6.	Semester	Second					
7.	Category of Course	DSE/PEC					
8.	Pre-requisite	VLSI Technology					

9.	Course Outcomes	<p>After completion of the course the students will be able to:</p> <p>CO1: Recall the basic principles of different sensors and actuators.</p> <p>CO2: Understand the process of miniaturization of a sensor and actuator.</p> <p>CO3: Apply various fabrication technologies for miniaturization of sensors and actuators for MEMS.</p> <p>CO4: Analyze the different properties of sensors and actuators.</p> <p>CO5: Evaluate the behaviour of MEMS devices.</p> <p>CO6: Create approaches for the designing of different MEMS based devices for various real-life applications.</p>
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10. Details of the Course

S. No.	Contents	Contact Hours
1.	Unit 1: Microfabrication and Micromachining: Integrated circuit processes, Bulk micromachining, Isotropic etching and anisotropic etching, Wafer bonding, High aspect-ratio processes, LIGA process.	10
2.	Unit 2: Physical Micro-Sensors: Classification of physical sensors, Integrated, Intelligent, Smart sensors, Sensor principles and examples: Thermal sensors, Electrical sensors, Mechanical sensors, Chemical and biosensors.	8
3.	Unit 3: Micro actuators: Electromagnetic and thermal micro-actuation, Mechanical design of micro actuators, Micro actuator examples, Microvalves, Micropumps, Micromotors Micro actuator systems, Success stories, Ink-Jet printer heads, Micro-Mirror TV projector.	8
4.	Unit 4: Surface Micromachining: One or two sacrificial layer processes, Surface micromachining requirements, Polysilicon surface micromachining, Other compatible	10

	<i>materials, Silicon dioxide, Silicon nitride, Piezoelectric materials, Surface micromachined systems: Success stories, Micromotors, Gear trains mechanisms.</i>	
5.	Unit 5: Application Areas: <i>All-mechanical miniature devices, 3-D electromagnetic actuators and sensors, RF/Electronics devices, Optical/Photonic devices, Medical devices E.G. DNA-chip, Micro-arrays. MEMS for RF applications: Need for RF MEMS components in communications, Space and defence applications</i>	9
	Total	45

11. Suggested Books

S. No.	Name of Authors/Books/Publishers	Edition	Year of Publication / Reprint
	Textbooks		
1.	Chang Liu, " Foundations of MEMS ", Pearson.	2 nd	2012
2.	Rai - Choudhury P., " MEMS and MOEMS Technology and Applications ", PHI Learning Private Limited.	1 st	2009
3.	Julian W. Gardner, " Microsensors, MEMS and Smart Devices ", Wiley.	1 st	2002
	Reference Books		
1.	Gabriel M. Rebeiz, " RF MEMS: Theory, Design, and Technology ", Wiley.	1 st	2003
2.	Stephen D. Senturia, " Microsystem design ", Springer.	1 st	2006

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GRAPHIC ERA (DEEMED TO BE UNIVERSITY), DEHRADUN

SEMESTER II

S. No.	Department of Electronics and Communication Engineering						
1.	Subject Code	VDM 242	Course Title		RF Integrated Circuits		
2.	Contact Hours	L	3	T	0	P	0
3.	Examination Duration	Theory		3	Practical		0
4.	Relative Weight	CIE	25	MSE	25	ESE	50
5.	Credit	03					
6.	Semester	Second					
7.	Category of Course	DSE/PEC					
8.	Pre-requisite	Electronics Devices and Circuits, Microwave Engineering					

9.	Course Outcomes	<p>After completion of the course the students will be able to:</p> <p>CO1: Recall the concepts of wireless technology in RF design</p> <p>CO2: Understand the modulation techniques for RF circuits.</p> <p>CO3: Apply the basics of detectors and transistor modelling, Mobile RF communication systems and basics of multiple access techniques.</p> <p>CO4: Analyse the concept of BJT and MOSFET behaviour at RF frequencies.</p> <p>CO5: Assess and evaluate Radio frequency devices.</p> <p>CO6: Design and develop RF based microelectronic devices.</p>
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10. Details of the Course

S. No.	Contents	Contact Hours
1.	Unit 1: Introduction: Introduction to RF and wireless technology: Complexity, Design and applications, Choice of technology. Basic concepts in RF design, Nonlinearly and time variance, Random processes and noise.	8
2.	Unit 2: Modulation Techniques for RF Circuits: Definition of sensitivity, Dynamic range, Conversion gains and distortion. Analog and Digital modulation for RF circuits: Comparison of various techniques for power efficiency. Coherent and non-coherent detection.	10
3.	Unit 3: Detectors and Transistor Modelling: Mobile RF communication systems and basics of multiple access techniques. Receiver and transmitter architectures and testing heterodyne, Homodyne, Image-reject, Direct-IF and sub-sampled receivers. Direct conversion and two steps transmitters. BJT and MOSFET behaviour at RF frequencies, Modelling of the transistors and SPICE models.	9
4.	Unit 4: Mixers and Oscillators:	10

	Noise performance and limitation of devices. Integrated parasitic elements at high frequencies and their monolithic implementation. Basic blocks in RF systems and their VLSI implementation: Low noise amplifiers design in various technologies, Design of mixers at GHz frequency range. Various mixers, Their working and implementations, Oscillators: Basic topologies VCO and definition of phase noise. Noise-power trade-off. Resonator less VCO design. Quadrature and single-sideband generators.	
5.	Unit 5: RF Synthesizer: Radio frequency synthesizers: PLL, Various RF synthesizer architectures and frequency dividers, Power amplifiers design. Linearization techniques, Design issues in integrated RF filters. Some discussion on available CAD tools for RF VLSI designs.	8
	Total	45

11. Suggested Books

S. No.	Name of Authors/Books/Publishers	Edition	Year of Publication / Reprint
	Textbooks		
1.	B. Razavi, “ RF Microelectronics ”, Prentice-Hall PTR.	2 nd	2012
2.	T. H. Lee, “ The Design of CMOS Radio-Frequency Integrated Circuits ”, Cambridge University Press.	1 st	1998
	Reference Books		
1.	R. Jacob Baker, H. W. Li, and D.E. Boyce, “ CMOS circuit design, Layout and simulation ”, Prentice-Hall of India.	1 st	1998

12.	Mode of Evaluation	Test / Quiz / Assignment / Mid Term Exam / End Term Exam
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GRAPHIC ERA (DEEMED TO BE UNIVERSITY), DEHRADUN

SEMESTER II

S. No.	Department of Electronics and Communication Engineering						
1.	Subject Code	VDM 243	Course Title		VLSI Circuits for Biomedical Application		
2.	Contact Hours	L	3	T	0	P	0
3.	Examination Duration	Theory		3	Practical		0
4.	Relative Weight	CIE	25	MSE	25	ESE	50
5.	Credit	03					
6.	Semester	Second					
7.	Category of Course	DSE/PEC					
8.	Pre-requisite	Advanced VLSI Circuit Design, CMOS Analog Circuit Design					

9.	Course Outcomes	<p>After completion of the course the students will be able to:</p> <p>CO1: Recall the concepts of neurochemical and neuro potential devices.</p> <p>CO2: Understand the mechanisms involved in the design of CMOS circuits for implantable biomedical devices and wireless biomedical applications.</p> <p>CO3: Analyze CMOS circuits for wireless medical application.</p> <p>CO4: Apply microneedles and their interfacing with neural systems.</p> <p>CO5: Evaluate the process of neuro-signal acquisition and amplification, neurochemical signal recording, and neuro stimulation.</p> <p>CO6: Develop CMOS circuits for biomedical applications.</p>
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10. Details of the Course

S. No.	Contents	Contact Hours
1.	Unit 1: Introduction: Wireless integrated neurochemical and neuropotential circuits: Introduction, Neurochemical sensing, Neuropotential sensing, RF telemetry and power harvesting in implanted devices, Multimodal electrical and chemical sensing. Visual cortical neuroprosthesis: A system approach: Introduction, System architecture, Prosthesis exterior body unit and wireless link, Body implantable unit, System prototype.	9
2.	Unit 2: CMOS Circuits for Biomedical Implantable Devices: Introduction, Inductive link to deliver power to implants, High data rate transmission through inductive links, Energy and bandwidth issues in multi-channel bio-potential recording. Towards self-powered sensors and circuits for biomedical implants: Introduction, Stress, Strain and fatigue	9

	<i>predication, In vivo strain measurement and motivation. Fundamental of piezoelectric-transduction and power delivery, Sub-microwatt piezo-powered VLSI circuits.</i>	
3.	Unit 3: CMOS Circuits for Wireless Medical Application: <i>Introduction, Spectrum regulations for medical use, Integrated receiver and transmitter architecture, Radio architecture, System budget, Low noise amplifier, Mixer, Polyphase filter, Power amplifier, PLL. Error correcting codes for in vivo RF wireless links.</i>	9
4.	Unit 4: Microneedles: <i>Introduction, Fabrication methods for hollowout-of-plane microneedles, Application for microneedles. Integrated circuit for neural interfacing: Introduction, nature of neural signals, Neural signal amplification.</i>	8
5.	Unit 5: Integrated Circuits for Neural Applications: <i>Integrated circuit for neural interfacing (Neurochemical recording), Integrated circuit for neural interfacing (Neural Stimulation): Introduction, Electrode configuration and tissue volume conductor, Electrode- Electrolyte Interface, Efficacy, Stimulus generator, Stimulation front end circuits.</i>	10
	Total	45

11. Suggested Books

S. No.	Name of Authors/Books/Publishers	Edition	Year of Publication / Reprint
	Textbooks		
1.	Kris Iniewski, “ VLSI Circuit Design for Biomedical Application ”, Artech House Publishers,	1 st	2008
2.	D. A. Hodges, H. G. Jackson and R. A. Saleh, “ Analysis and Design of Digital Integrated Circuits in Deep Submicron Technology ”, Tata McGraw-Hill.	3 rd	2003
	Reference Books		
1.	Parag. K. Lala, “ Digital circuit testing and testability ”, Academic Press.	1 st	1997
2.	Ashok K. Sharma, “ Semiconductor memories technology, testing and reliability ”, Prentice-Hall of India Private Limited.	1 st	2002

12.	Mode of Evaluation	Test / Quiz / Assignment / Mid Term Exam / End Term Exam
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GRAPHIC ERA (DEEMED TO BE UNIVERSITY), DEHRADUN

SEMESTER II

S. No.	Department of Electronics and Communication Engineering						
1.	Subject Code	VDM 244	Course Title		Microwave & MM-wave Integrated Circuits and Applications		
2.	Contact Hours	L	3	T	0	P	0
3.	Examination Duration	Theory		3	Practical		0
4.	Relative Weight	CIE	25	MSE	25	ESE	50
5.	Credit	03					
6.	Semester	Second					
7.	Category of Course	DSE/ PEC					
8.	Pre-requisite	Microwave Engineering					

9.	Course Outcomes	<p>After completion of the course the students will be able to:</p> <p>CO1: Describe the requirement of MMIC and MM-wave technologies and their various applications.</p> <p>CO2: Understand the fabrication processes Circuit of Microwave Integrated MIC.</p> <p>CO3: Implement the various active and passive circuit elements for microwave and MM-wave technology.</p> <p>CO4: Analyze the various measurement systems using MM-wave technology.</p> <p>CO5: Evaluate the microwave components for designing microwave Integrated circuits.</p> <p>CO6: Design of MMIC using MM-Wave Technology.</p>
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10. Details of the Course

S. No.	Contents	Contact Hours
1.	Unit 1: Introduction: Introduction to Monolithic Microwave Integrated Circuits (MMICs) technology, different types of MMIC, Advantages disadvantages and application of MMICs, MMIC fabrication techniques, Thick and thin film technologies and materials, Encapsulation and mounting of active devices, Introduction to MM-wave integrated circuits, GaAs fabrication technology and various processes, Materials used for MM-wave integrated guides.	10
2.	Unit 2: Passive components: Introduction, Inductors, Capacitors, Resistors, Via-holes, and grounding, Microstrip components, Coplanar circuits, Multilayer techniques, Micromachined passive components.	10
3.	Unit 3: Active Semiconductor circuit elements:	10

	Active device technologies and design approaches, Fabrication and modeling: Bipolar junction transistor, Hetero junction bipolar transistor, High electron mobility transistor, MESFET, CMOS, BiCMOS.	
4.	Unit 4: Measurement Techniques: Introduction, Test fixture measurements, Probe station measurements, Thermal and cryogenic measurements, Experimental field probing techniques, MM-wave measurement techniques: Electric field probe, Measurement of attenuation constant and guide wavelength. Measurement at radiation loss at bends.	9
5.	Unit 5: System Application: MICs in phased array radars, MICs in satellite television systems, Microwave radio systems, Monolithic MM-wave transceiver.	6
	Total	45

11. Suggested Books

S. No.	Name of Authors/Books/Publishers	Edition	Year of Publication / Reprint
	Textbooks		
1.	I. D. Robertson and S. Lucyszyn, “ RFIC and MMIC design and technology ”, The Institute of Electrical Engineers.	2 nd	2001
2.	Leo G. Maloratsk, “ Passive RF and Microwave Integrated Circuits ”, Elsevier.	1 st	2004
3.	K. C. Gupta and A. Singh, “ Microwave Integrated circuit ”, John Wiley & Sons.	2 nd	1974
4.	E. Carey and S. Lidholm, “ Millimeter wave Integrated Circuit ”, Springer.	2 nd	2005
	Reference Books		
1.	I. Kneppo, J. Fabian, P. Bezousek, P. Hrnicko and M. Pavel, “ Microwave Integrated Circuits ”, John Wiley & Sons	1 st	1994
2.	S. K. Koul, “ Millimeter Wave and Optical Dielectric Integrated Guides and Circuits ”, John Wiley & Sons.	1 st	1997
3.	Duixian Liu, Ulrich Pfeiffer, Janusz Grzyb and Brian Gaucher, “ Advanced Millimeter-wave Technologies: Antennas, Packaging and Circuits ”, Wiley.	1 st	2009

12.	Mode of Evaluation	Test / Quiz / Assignment / Mid Term Exam / End Term Exam
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GRAPHIC ERA (DEEMED TO BE UNIVERSITY), DEHRADUN

SEMESTER III

S. No.	Department of Electronics and Communication Engineering						
1.	Subject Code	VDM 341	Course Title		Organic Electronics Devices and Circuits		
2.	Contact Hours	L	3	T	0	P	0
3.	Examination Duration	Theory		3	Practical		0
4.	Relative Weight	CIE	25	MSE	25	ESE	50
5.	Credit	03					
6.	Semester	Third					
7.	Category of Course	DSE/PEC					
8.	Pre-requisite	Basic Electronics Engineering, Electronics Devices and Circuits.					

9.	Course Outcomes	<p>After completion of the course the students will be able to:</p> <p>CO1: Ability to describe basic concepts and limitations of conventional silicon-based semiconductor devices.</p> <p>CO2: Understand the basic concepts and classification of organic materials.</p> <p>CO3: Apply the advancement of charge transport in organic materials for different organic electronic devices.</p> <p>CO4: Design and develop innovative organic electronic devices.</p> <p>CO5: Evaluate the performance of organic solar cells.</p> <p>CO6: Analyse the different properties of OLED.</p>
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10. Details of the Course

S. No.	Contents	Contact Hours
1.	Unit 1: Organic Materials and Device Physics: Introduction; Organic materials: Conducting polymers and small molecules, Organic semiconductors: p-type and n-type semiconductors, Source, Drain and Gate electrodes, Gate dielectrics, Substrate. Energy band diagram and concept of charge transport in organic semiconductors; Comparison between organic and inorganic semiconductors including the merits, Demerits and limitations.	10
2.	Unit 2: Organic Thin Film Transistors (OTFTs): Introduction; Operating principle; Output and transfer characteristics; Classification of various organic thin film transistors (OTFT) structures; Performance parameters; Impact of structural parameters on behaviour of OTFT; Concept of contact resistance; Single Gate (SG) and Dual Gate (DG) TFT performance comparison; Merits, Demerits, Limitations and	8

	future scope. Applications: - Organic complementary inverter circuits; Organic memory - Organic static random-access memory (OSRAM).	
3.	Unit 3: Organic Light Emitting Diodes (OLEDs) Introduction; Organic materials for OLEDs; Classification of OLEDs, Operating principle; Output and transfer characteristics; Analysis of OLED performance: Optical, Electrical and thermal properties, Merits and demerits; Stability issues; OLEDs as display applications.	8
4.	Unit 4: Organic Solar Cell: Introduction; Operating principle; Characteristics; Materials for organic solar cells; Classification of organic solar cell- Single layer, Bi-layer and bulk hetero junction organic solar cell; Merits and demerits; Applications and future scope.	9
5.	Unit 5: Organic Sensors: Introduction; Working principle and organic sensing materials for pressure sensors (Piezoresistive, Piezoelectric, and Capacitive sensor), Temperature sensors, Humidity sensors and pH sensor; comparison between organic and conventional sensors including merits, demerits and limitations; Applications of organic sensors; Basics of ionic polymer-metal composites (IPMC) and its applications.	10
	Total	45

11. Suggested Books

S. No.	Name of Authors/Books/Publishers	Edition	Year of Publication / Reprint
	Textbooks		
1.	Hagen Klauk, " Organic Electronics: Materials, Manufacturing and Applications ", Wiley-VCH VerlagGmbH & Co. KGaA, Germany.	1 st	2006
2.	Klaus Mullen, Ullrich Scherf, " Organic Light Emitting Devices: Synthesis, Properties and Applications ", Wiley-VCH VerlagGmbH & Co. KGaA, Germany..	1 st	2002
3.	Johannes Karl Fink, " Polymeric Sensors and Actuators ", John Wiley & Sons.	1 st	2012
	Reference Books		
1.	Hagen Klauk, " Organic Electronics II: More Materials and Applications ", Wiley-VCH VerlagGmbH & Co. KGaA, Weinheim, Germany.	1 st	2012
2.	Flora Li, Arokia Nathan, Yiliang Wu, Beng S. Ong, " Organic Thin Film Transistor Integration: A Hybrid Approach ", Wiley-VCH, Germany.	1 st	2011
3.	Wolfgang Brütting, " Physics of Organic Semiconductors ", Wiley-VCH VerlagGmbH & Co. KGaA, Germany.	2 nd	2005
4.	Daniel A. Bernards, Róisín M. Owens, George G. Malliaras, " Organic Semiconductors in Sensor Applications ", Springer Science & Business Media.	1 st	2008

12.	Mode of Evaluation	Test / Quiz / Assignment / Mid Term Exam / End Term Exam
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GRAPHIC ERA (DEEMED TO BE UNIVERSITY), DEHRADUN

SEMESTER III

S. No.	Department of Electronics and Communication Engineering						
1.	Subject Code	VDM 342	Course Title		Memory Design and Testing		
2.	Contact Hours	L	3	T	0	P	0
3.	Examination Duration	Theory		3	Practical		0
4.	Relative Weight	CIE	25	MSE	25	ESE	50
5.	Credit	03					
6.	Semester	Third					
7.	Category of Course	DSE/PEC					
8.	Pre-requisite	Low Power VLSI Design					

9.	Course Outcomes	<p>After completion of the course the students will be able to:</p> <p>CO1: Acquire the fundamental knowledge of CMOS memory devices.</p> <p>CO2: Infer about configuration of fundamental VLSI chip.</p> <p>CO3: Ability to implement high performance digital VLSI memory systems.</p> <p>CO4: Analyze different techniques required to implement low power memory chip.</p> <p>CO5: Evaluate the characteristics of digital VLSI memory systems.</p> <p>CO6: Design of low power memory devices.</p>
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10. Details of the Course

S. No.	Contents	Contact Hours
1.	<p>Unit 1: Introduction to Memory Chip Design:</p> <p>Basics of Semiconductor Memory, Internal Organization of Memory Chips, Memory Cell Array, Peripheral Circuit, I/O Interface Categories of Memory Chip, History of Memory-Cell Development, Architectures of memory cell: SRAM Cell, DRAM Cell Trends in Non-Volatile Memory Design and Technology, Ferroelectric memory, Basic Operation of Flash Memory Cells, Advances in Flash-Memory Design and Technology.</p>	10
2.	<p>Unit 2: Basics of RAM Design and Technology:</p> <p>Devices, NMOS Static Circuits, NMOS Dynamic Circuits, CMOS Circuits, Basic Memory Circuits, Scaling Law.</p> <p>On-Chip Voltage Generators:</p> <p>Substrate-Bias Voltage (VBB) Generator, Voltage Up Converter, Voltage Down-Converter, Half-VDD Generator, Examples of Advanced On-Chip Voltage Generators.</p>	8
3.	Unit 3: DRAM Circuits:	8

	<i>High-Density Technology, High-Performance Circuits, Catalog Specifications of the Standard DRAM, Basic Configuration and Operation of the DRAM Chip, Chip Configuration, Address Multiplexing, Fundamental Chip, Multi-divided Data Line and Word Line, Read and Relevant Circuits, Write and Relevant Circuits, Refresh-Relevant Circuits, Redundancy Techniques, On-Chip Testing Circuits, High Signal-to-Noise Ratio DRAM Design and Technology, Trends in High S/N Ratio Design, Data-Line Noise Reduction, Noise Sources.</i>	
4.	Unit 4: High-Performance Subsystem Memories: <i>Hierarchical Memory Systems, Memory-Subsystem Technologies, High-Performance Standard DRAMs, Embedded Memories. Low-Power Memory Circuits: Sources and Reduction of Power Dissipation in a RAM Subsystem and Chip, Low-Power DRAM Circuits, Low-Power SRAM Circuits.</i>	10
5.	Unit 5: Ultra-Low-Voltage Memory Circuits: <i>Design Issues for Ultra-Low-Voltage RAM Circuits, Reduction of the Subthreshold Current, Stable Memory-Cell Operation, Suppression of, or Compensation for, Design Parameter Variations, Power-Supply Standardization, Ultra-Low Voltage DRAM Circuits, Ultra-Low-Voltage SRAM Circuits, Ultra-Low-Voltage SOI Circuits.</i>	9
	Total	45

11. Suggested Books

S. No.	Name of Authors/Books/Publishers	Edition	Year of Publication / Reprint
	Textbooks		
1.	Itoh, K., “ VLSI Memory Chip Design ”, Springer,	3 rd	2006
2.	Sharma, A. K., “ Semiconductor Memories: Technology, Testing and Reliability ”, Wiley- IEEE press.	1 st	2002
	Reference Books		
1.	J. B. Kuo and J. H. Lou, Low “ Voltage CMOS VLSI Circuits ”, Wiley.	1 st	1999
2.	J. M. Rabaey, A. P. Chandrakasan and B. Nikolic, “ Digital Integrated Circuits: A Design Perspective ”, Pearson Education.	2 nd	2003

12.	Mode of Evaluation	Test / Quiz / Assignment / Mid Term Exam / End Term Exam
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GRAPHIC ERA (DEEMED TO BE UNIVERSITY), DEHRADUN

SEMESTER III

S. No.	Department of Electronics and Communication Engineering						
1.	Subject Code	VDM 343	Course Title		System on Chip Design and Testing		
2.	Contact Hours	L	3	T	0	P	0
3.	Examination Duration	Theory		3	Practical		0
4.	Relative Weight	CIE	25	MSE	25	ESE	50
5.	Credit	03					
6.	Semester	Third					
7.	Category of Course	DSE/PEC					
8.	Pre-requisite	VLSI Technology					

9.	Course Outcomes	<p>After completion of the course the students will be able to:</p> <p>CO1: Recall the concepts of System-On-Chip (SoC) Testing.</p> <p>CO2: Understand the concepts of digital test architectures design.</p> <p>CO3: Apply the concepts of SoC on delay testing and low-power testing.</p> <p>CO4: Analyze the basics of system/network-on-chip test architectures.</p> <p>CO5: Assess and evaluate debug and diagnosis.</p> <p>CO6: Implement different testing techniques in SoC.</p>
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10. Details of the Course

S. No.	Contents	Contact Hours
1.	<p>Unit 1: Introduction:</p> <p>Importance of system-on-chip testing, Basics of SoC testing, Basics of memory testing, SoC design examples.</p> <p>Digital Test Architectures: Scan design, Logic built-In self-test, Test compression, Random-access scan design.</p> <p>Fault-Tolerant Design: Fundamentals of fault tolerance, Fundamentals of coding theory, Fault tolerance schemes</p>	8
2.	<p>Unit 2: System/Network-on-Chip Test Architectures:</p> <p>System-on-Chip (SoC) testing, Network-on-Chip (NoC) testing, Design and test practice: Case studies.</p> <p>SIP Test Architectures: Introduction, Bare die, Functional system test, Test of embedded components.</p> <p>Delay Testing: Delay test application, Delay fault models, Delay test sensitization, Delay fault, Delay fault test generation, Pseudo-functional testing to avoid over-testing</p>	9
3.	Unit 3: Low-Power Testing:	8

	<p><i>Introduction, Energy and power modelling, Test power issues, Low-power scan testing, Low-power built-in self-test, Low-power test data compression, Low-power RAM testing.</i></p> <p><i>Coping with Physical Failures, Soft Errors, and Reliability Issues:</i> <i>Signal integrity, Manufacturing defects, Process variations, and Reliability, Soft errors, Defect and error tolerance.</i></p>	
4.	<p><i>Unit 4: Design for Manufacturability and Yield:</i> <i>Introduction, Yield, components of yield, Photolithography, DFM and DFY, Variability, Metrics for DFX.</i></p> <p><i>Design for Debug and Diagnosis:</i> <i>Introduction to logic design for debug and diagnosis (DFD) structures, Probing technologies, Circuit editing, Physical DFD structures, Diagnosis and debug process.</i></p>	10
5.	<p><i>Unit 5: Software-Based Self-Testing:</i> <i>Introduction, Software-based self-testing paradigm, Processor functional fault self-testing, Processor structural fault self-testing, Processor self-diagnosis, testing global interconnect, testing nonprogrammable cores, Instruction-level DFT, DSP-Based Analog/Mixed-signal component testing.</i></p> <p><i>Field Programmable Gate Array Testing:</i> <i>Overview of FPGAs, Testing approaches, BIST of programmable resources, Embedded processor-based testing</i></p>	10
	Total	45

11. Suggested Books

S. No.	Name of Authors/Books/Publishers	Edition	Year of Publication / Reprint
	Textbooks		
1.	Laung-Terng Wang, Charles E. Stroud, Nur A. Touba, “ System-On-Chip Test Architectures (Nanometer Design for Testability) ”. Elsevier.	1 st	2008
	Reference Books		
1.	Erik Larsson, “ Introduction to Advanced system- on- chip test design and optimization ”, Springer.	5 th	2006

12.	Mode of Evaluation	Test / Quiz / Assignment / Mid Term Exam / End Term Exam
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GRAPHIC ERA (DEEMED TO BE UNIVERSITY), DEHRADUN

SEMESTER III

S. No.	Department of Electronics and Communication Engineering						
1.	Subject Code	VDM 344	Course Title		Internet of things		
2.	Contact Hours	L	3	T	0	P	0
3.	Examination Duration	Theory		3	Practical		0
4.	Relative Weight	CIE	25	MSE	25	ESE	50
5.	Credit	03					
6.	Semester	Second					
7.	Category of Course	DSE/PEC					
8.	Pre-requisite	Fundamentals of Computer and Programming Language					

9.	Course Outcomes	<p>After completion of the course the students will be able to:</p> <p>CO1: Explain the terms used in IoT</p> <p>CO2: Describe key technologies in Internet of Things</p> <p>CO3: Identify components needed to provide a solution for certain applications</p> <p>CO4: Analyze security requirements in an IoT system</p> <p>CO5: Design wireless sensor network architecture and its framework along with WSN applications</p> <p>CO6: Understand business models for the Internet of Things</p>
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10. Details of the Course

S. No.	Contents	Contact Hours
1.	Unit1: INTRODUCTION: Introduction to Internet of Things: History of IoT, About IoT, Overview and Motivations, Examples of Applications, Internet of Things Definitions and Frameworks: IoT Definitions, IoT Architecture, General Observations, ITUT Views, Working Definition, IoT Frameworks, Basic Nodal Capabilities.	8
2.	Unit 2: FUNDAMENTAL IoT MECHANISMS AND KEY TECHNOLOGIES: Identification of IoT Objects and Services, Structural Aspects of the IoT, Environment Characteristics, Traffic Characteristics, Scalability, Interoperability, Security and Privacy, Open Architecture, Key IoT Technologies, Device Intelligence, Communication Capabilities, Mobility Support, Device Power, Sensor Technology, RFID Technology, Satellite Technology.	10
3.	Unit 3: RADIO FREQUENCY IDENTIFICATION TECHNOLOGY RFID: Introduction, Principle of RFID, Components of an RFID system, Issues EPCGlobal Architecture Framework: EPCIS & ONS, Design issues, Technological challenges, Security challenges, IP for IoT, Web of Things.	10

	Wireless Sensor Networks: History and context, WSN Architecture, the node, Connecting nodes, Networking Nodes, Securing Communication WSN specific IoT applications, challenges: Security, QoS, Configuration, Various integration approaches, Data link layer protocols, routing protocols and infrastructure establishment.	
4.	Unit 4: RESOURCE MANAGEMENT IN THE INTERNET OF THINGS: Clustering, Software Agents, Clustering Principles in an Internet of Things Architecture, Design Guidelines, and Software Agents for Object Representation, Data Synchronization. Identity portrayal, Identity management, various identity management models: Local, Network, Federated and global web identity, user-centric identity management, device centric identity management and hybrid-identity management, Identity and trust.	8
5.	Unit 5: INTERNET OF THINGS PRIVACY, SECURITY AND GOVERNANCE: Vulnerabilities of IoT, Security requirements, Threat analysis, Use cases and misuse cases, IoT security tomography and layered attacker model, Identity establishment, Access control, Message integrity, Non-repudiation and availability, Security model for IoT. Internet of Things Application: Smart Metering Advanced Metering Infrastructure, e-Health Body Area Networks, City Automation, Automotive Applications, Home Automation, Smart Cards.	9
	Total	45

11. Suggested Books

S. No.	Name of Authors/Books/Publishers	Edition	Year of Publication / Reprint
	Textbooks		
1.	Daniel Minoli, “ Building the Internet of Things with IPv6 and MIPv6: The Evolving World of M2M Communications ”, Willy Publications	1 st	2013
2.	Bernd Scholz-Reiter, Florian Michahelles, “ Architecting the Internet of Things ”, Springer	1 st	2011
3.	Parikshit N. Mahalle&Poonam N. Railkar, “ Identity Management for Internet of Things ”, River Publishers	1 st	2015
	Reference Books		
1.	Samuel Greengard, “ The Internet of Things ”, Simon & Schuster Publisher	1 st	2014
2.	Timothy Chou, “ Precision: Principles, Practices and Solutions for the Internet of Things ”, O'Reilly Media	2 nd	2017

12.	Mode of Evaluation	Test / Quiz / Assignment / Mid Term Exam / End Term Exam
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12. Program Articulation Matrix



13. EXIT OPTIONS:

SEMESTER	Exit Option	Credits
I & II	Post-Graduate Diploma in VLSI Design and Systems	40
III & IV	M. Tech in VLSI Design and Systems	40

14. List of Potential Recruiters for Employing Graduates in Electronics and Communication Engineering

- Microsoft Corporation
- Apps Associates
- Google
- Acuity Knowledge
- Adobe
- LTTS
- Amazon
- LTIMindtree
- Walmart Global Technology
- IBM
- Coforge
- Zscaler
- TCS
- Goldman Sachs
- Infosys
- Latent View
- Capgemini
- Bonami Software
- HCL
- Incture
- Informatica
- ANM
- Teradata
- Wissen Technologies
- EY India
- DXC
- 75Way Technologies
- Contata
- Global Logic
- Sopra Steria
- PWC
- MAQ Software
- Enquero Global
- Intel
- HSBC
- Hexaware Technology
- Accenture
- Yamaha
- Accolite
- JSW
- Cognizant
- Autopay
- Vinculum
- Nineleaps
- Atlassian
- American Express
- Airbus India
- Salesforce
- Tally India
- Lowes India
- Morgan Stanley
- AbinBevGCC
- Flipkart
- Siemens
- L&T Infotech
- Deloitte
- Samsung Electronics
- Godrej Electronics
- Mentor Graphics
- STMicroelectronics and Many more