GRAPHIC ERA (DEEMED TO BE UNIVERSITY), DEHRADUN
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING
TIME TABLE (Offline), M.TECH (VLSI Design and Systems), Sem-III

Classroom: EC Lab-03 (Cadence Lab) **w.e.f. July 21, 2025**

Time/ Day	10:10 AM- 11:05 AM	11:05 AM- 12:00 PM	12:00 PM- 12:55 PM	12:55 PM- 1:55 PM	1:55 PM- 2:50 PM	3:10 PM- 4:05 PM	4:05 PM- 5:00 PM
MON	Dissertation Phase- I			LUNCH	VDM 301	VDM 302	VDM 391
TUE	Dissertation Phase- I				VDM 391	VDM 302	VDM 303
WED	Dissertation Phase- I				VDM 391	VDM 351	
THU	Dissertation Phase- I				VDM 301	VDM 351	
FRI	Dissertation Phase- I				VDM 301	VDM 303	

Class Coordinator: Dr. Gaurav Verma

Code	Subject	Concerned Faculty	Load (L.T.P)
VDM 391	Organic Electronics Devices and Circuits	Prof. (Dr.) Varij Panwar	3-0-0
VDM 301	VLSI Physical Design Automation	Mr. Kamlesh Kukreti	3-0-0
VDM 302	Research Methodology and IPR	Prof. (Dr.) Santosh Shankarrao Saraf	2-0-0
VDM 303 (Through Swayam)	C-Based VLSI Design (Through Swayam)	Prof. (Dr.) Gourav Verma	3-0-0
Laboratories			
VDM 351	Modeling and Simulation Lab	Mr. Kamlesh Kukreti	0-0-4
VDM 352	Dissertation Phase- I	Prof. (Dr.) Varij Panwar	0-0-20

Dr. Kaushal Kumar
Timetable Coordinator

Prof. (Dr.) Md. Irfanul Hasan
HOD (ECE)