GRAPHIC ERA (DEEMED TO BE UNIVERSITY), DEHRADUN
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING
TIMETABLE (Offline), M. TECH (VLSI Design and Systems), Sem-II Rev :01

Classroom: Project Lab **w.e.f. 3rd February 2025**

Time/ Day	9:00 AM- 9:55 AM	09:55AM- 10:50 AM	11:10 AM- 12:05 PM	12:05 PM- 1:00PM	1:00 PM- 1:55 PM	1:55 PM- 2:50 PM	2:50 PM- 3:45 PM	4:00 PM- 4:55 PM
MON	VDM 202	VDM 252		VDM 241	LUNCH	VDM 253		Library
TUE	VDM 204	VDM 241	VDM 203	VDM 201		VDM 251		Library
WED	VDM 202	VDM 251		VDM 203		VDM 253		VDM 204
THU	VDM 201	VDM 241	VDM 203	VDM 202		VDM 202	VDM 204	Library
FRI	VDM 201	VDM 203	VDM 252			VDM 241	VDM 204	VDM 201

Class Coordinator: Mr. Kamlesh Kukreti

Code	Subject:	Concerned Faculty:	Load (L.T.P)
VDM 201	Advanced ASIC and FPGA Design	Mr. Kamlesh Kukreti	3-0-0
VDM 202	Digital System Design using Verilog HDL	Dr. Abhay Sharma	3-0-0
VDM 203	Advanced VLSI Circuit Testing	Ms. Alankrita Joshi	3-0-0
VDM 204	Low Power VLSI Design	Dr. Gourav Verma	3-0-0
VDM 241	Micro-Sensors and MEMS	Prof. (Dr.) Varij Panwar	3-0-0
Laboratories			
VDM 251	Verilog HDL Lab	Dr. Abhay Sharma	0-0-2
VDM 252	VLSI Physical Design Lab	Mr. Kamlesh Kukreti	0-0-2
VDM 253	Mini Project with Seminar	Dr. Gourav Verma	0-0-2

Dr. Kaushal Kumar
Timetable Coordinator

Prof. (Dr.) Md. Irfanul Hasan
HOD (ECE)