GRAPHIC ERA (DEEMED TO BE UNIVERSITY), DEHRADUN
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING
TIMETABLE (Offline), M. TECH (VLSI Design and Systems), Sem-IV

w.e.f. 27th January 2025

Time/ Day	08:00AM-08:55AM	08:55AM-9:50 AM	10:10AM-11:05M	11:05 AM-12:00 PM	12:00 PM-1:00PM	1:00 PM-1:55 PM	1:55PM-2:50PM	3:10 PM-4:05 PM
MON	Dissertation Phase-II					LUNCH	Dissertation Phase-II	
TUE	Dissertation Phase-II						Dissertation Phase-II	
WED	Dissertation Phase-II						Dissertation Phase-II	
THU	Dissertation Phase-II						Dissertation Phase-II	
FRI	Dissertation Phase-II						Dissertation Phase-II	

Class Coordinator: Prof. (Dr.) Varij Panwar

Code	Subject:	Concerned Faculty:	Load (L.T.P)
VDM 401	Dissertation Phase-II	Prof. (Dr.) Varij Panwar	0-0-28

Dr. Kaushal Kumar
Timetable Coordinator

Prof. (Dr.) Md. Irfanul Hasan
HOD (ECE)