

**GRAPHIC ERA (DEEMED TO BE UNIVERSITY), DEHRADUN**  
**DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING**  
**TIMETABLE (Revised I), M. TECH (VLSI Design and Systems), Sem-II**

Classroom: Cadence Lab

w.e.f. 4<sup>th</sup> March 2024

Time/ Day	09:00AM- 9:55 AM	09:55AM- 10:50 AM	11:10 AM- 12:05 PM	12:05 PM- 1:00PM	1:00 PM- 1:55 PM	1:55PM- 2:50PM	3:10 PM- 4:05 PM	4:05 PM- 05:00 PM
<b>MON</b>	VDM 204	VDM 252		VDM 291	LUNCH	VDM 253		Library
<b>TUE</b>	VDM 204	VDM 201	VDM 202	VDM 203	LUNCH	VDM 253		Library
<b>WED</b>	VDM 203	VDM 252		LUNCH	VDM 202	VDM 251		VDM 204
<b>THU</b>	VDM 201	VDM 291	VDM 202	VDM 203	LUNCH	VDM 291	VDM 204	Library
<b>FRI</b>	VDM 201	VDM 203	VDM 251		LUNCH	VDM 201	VDM 202	VDM 291

Class Coordinator: Mr. Kamlesh Kukreti

Code	Subject:	Concerned Faculty:	Load (L.T.P)
VDM 201	Advanced ASIC and FPGA Design	Mr. Kamlesh Kukreti	3-0-0
VDM 202	Digital System Design using Verilog HDL	Dr. Abhay Sharma	3-0-0
VDM 203	Advanced VLSI Circuit Testing	Dr. Varun Mishra	3-0-0
VDM 204	Low Power VLSI Design	Ms. Alankrita Joshi	3-0-0
VDM 291	Micro-Sensors and MEMS	Dr. Varij Panwar	3-0-0
<b>Laboratories</b>			
VDM 251	Verilog HDL Lab	Ms. Alankrita Joshi	0-0-2
VDM 252	VLSI Physical Design Lab	Mr. Kamlesh Kukreti	0-0-2
VDM 253	Mini Project with Seminar	Dr. Varij Panwar	0-0-2

Dr. Vinay Kumar  
**Timetable Coordinator**

Prof. (Dr.) Md. Irfanul Hasan  
**HOD (ECE)**