GRAPHIC ERA (DEEMED TO BE UNIVERSITY), DEHRADUN
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING
TIMETABLE (Revised), M. TECH (VLSI Design and Systems), Sem-I

Classroom: Cadence Lab **w.e.f. September 9, 2023**

Time/ Day	08:00AM-08:55AM	08:55AM-9:50 AM	10:10AM-11:05M	11:05 AM-12:00 PM	12:00 PM-1:00PM	1:00 PM-1:55 PM	1:55PM-2:50PM	3:10 PM-4:05 PM
MON	VDM 151		VDM 104	VDM 101	VDM 191	LUNCH	Research Activity	
TUE	VDM 102	VDM 102	VDM 103	VDM 191	VDM 104	LUNCH	Library	
WED	VDM 101	VDM 151		VDM 191	LUNCH	VDM 103	VDM 104	Library
THU	VDM 102	VDM 101	VDM 191	VDM 103	LUNCH	VDM 104	VDM 152	
FRI	VDM 103	VDM 152		VDM 102	LUNCH	VDM 101	Research Activity	

Class Coordinator: Mr. Kamlesh Kukreti

Code	Subject:	Concerned Faculty:	Load (L.T.P)
VDM 101	Semiconductor Materials and Devices	Dr. Peyush Pande	3-0-0
VDM 102	CMOS Analog Circuit Design	Dr. Chandni Tiwari	3-0-0
VDM 103	Advanced Digital Integrated Circuit	Mr. Kamlesh Kukreti	3-0-0
VDM 104	VLSI Technology	Prof. (Dr.) Santosh Saraf	3-0-0
VDM 191	Advanced Nanotechnology	Dr. Varij Panwar	3-0-0
Laboratories			
VDM 151	CMOS Analog Circuit Design Lab	Dr. Varun Mishra	0-0-2
VDM 152	Digital VLSI Circuit Lab	Mr. Kamlesh Kukreti	0-0-2

Dr. Vinay Kumar
Timetable Coordinator

Prof. (Dr.) Md. Irfanul Hasan
HOD (ECE)