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NOTICE

Department of Electronics and Communication Engineering

Schedule of External Practical Examination

IInd Semester

Date- 06-06-2023

This is to inform all students of M.Tech(VLSI Design and Systems), IInd Semester that their external practical examinations are as per following schedule. It is directed that all the students carry admit card and must report on time with completely checked and binded practical file.

S.No	Subject Name and Code	Date	Time	Lab Incharge
1	Verilog HDL Lab (VDM 251)	12 th June,2023	9:00am onwards	Mrs. Alankrita Joshi
2	VLSI Physical Design Lab (VDM 252)	13 th June,2023	9:00am onwards	Mr. Kamlesh Kukreti
3	Mini Project with Seminar (VDM 253)	14 th June,2023	9:00am onwards	Dr. Chandni Tiwari

*Note- All students are requested to submit their seminar report and power point presentation before presentation starts.

Kamlesh Kukreti

Class Coordinator

Prof. (Dr.) Md. Irfanul Hasan

HoD, ECE