GRAPHIC ERA (DEEMED TO BE UNIVERSITY), DEHRADUN
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING
TIME TABLE (Offline), M.TECH (VLSI Design and Systems), Sem-II

Classroom: Project Lab **w.e.f. 8th May 2023**

Time/ Day	09:00AM-9:55 AM	9:55 AM - 10:50AM	11:10 AM-12:05 AM	12:05 PM-1:00PM	1:00 PM-1:55 PM	1:55PM-2:50PM	3:10 PM-4:05 PM	4:05 PM-5:00 PM
MON				VDM 203 (Lab 3)	VDM 253		Library	Library
TUE	VDM 201	VDM 203	VDM 202	**LUNCH**	VDM 252		VDM 204	VDM 291
WED	VDM 251		VDM 202	VDM 291	**LUNCH**	VDM 203 (Lab 3)	VDM 204	Library
THU	VDM 201	VDM 252		VDM 291	**LUNCH**	VDM 204	Library	Library
FRI	VDM 203	VDM 291	VDM 201	**LUNCH**	VDM 202	VDM 204	Library	Library
SAT	VDM 201	VDM 251		**LUNCH**	VDM 202	VDM 253		Library

Class Coordinator: Mr. Kamlesh Kukreti

Code	Subject:	Concerned Faculty:	Load (L.T.P)
VDM 201	Advanced ASIC and FPGA Design	Mr. Kamlesh Kukreti	3-0-0
VDM 202	Digital System Design using Verilog HDL	Ms. Alankrita Joshi	3-0-0
VDM 203	Advanced VLSI Circuit Testing	Dr. Chandni Tiwari	3-0-0
VDM 204	Low Power VLSI Design	Dr. U. M. Bhatt	3-0-0
VDM 291	Micro-Sensors and MEMS	Dr. Varij Panwar	3-0-0
Laboratories			
VDM 251	Verilog HDL Lab	Ms. Alankrita Joshi	0-0-2
VDM 252	VLSI Physical Design Lab	Mr. Kamlesh Kukreti	0-0-2
VDM 253	Mini Project with Seminar	Dr. Chandni Tiwari	0-0-2

Dr. Vinay Kumar
Timetable Coordinator

Prof. (Dr.) Md. Irfanul Hasan
HOD (ECE)