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Department of Electronics and Communication Engineering

Kind attention to M. Tech (VLSI Design and Systems)

End Semester Practical Exam Schedule (Ist Semester)

March 10, 2021

Notice

End semester VLSI HDL Lab (VDM 151) and Digital VLSI Circuit Lab (VDM-152) examination has been scheduled on 19th March 2021 and 20th March 2021, respectively. Students must maintain the following schedule:

Date	Time of Examination	Lab Name
19-03-2021	11:00am to 01:00pm	VLSI HDL Lab (VDM 151)
20-03-2021	02:30pm to 04:30pm	Digital VLSI Circuit Lab (VDM-152)

Note: Every student must bring 'lab record file' checked by the concerned faculty member.

10/3/2021

Lab In charge

HoD

Dept of ECE