

# GRAPHIC ERA UNIVERSITY DEHRADUN

## Semester VIII

Name of Department: - **Electronics and Communication Engineering**

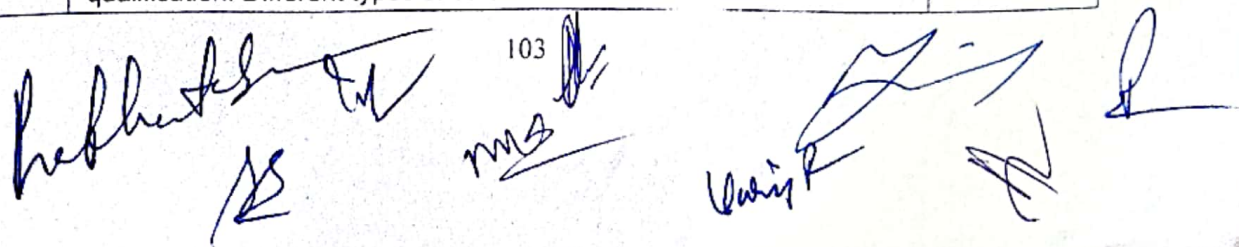
1. Subject Code: **TEC 801** Course Title: **Satellite Communication**
2. Contact Hours: L: **3** T: **1** P: **0**
3. Examination Duration (Hrs): Theory **3** Practical **0**
4. Relative Weight: CWS **25** PRS **0** MTE **25** ETE **50** PRE **0**
5. Credits: **4**
6. Semester: **Spring (Even)**
7. Subject Area: **Core**
8. Pre-requisite: **None**

<b>9. Course Outcomes:</b>	<ul style="list-style-type: none"> <li>Good knowledge of the field.</li> <li>A clear understanding of the various subsystems used in satellite communication and navigation as well.</li> <li>Satellite link design analysis.</li> <li>Different satellite Multiple Access Techniques.</li> <li>To make the student competent to face the tough selection criteria of R &amp; D organizations in India and abroad.</li> </ul>
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### 10. Details of the Course:

Sl. No.	Contents	Contact Hours
1	<b>Overview of Satellite Systems, Orbits and Launching Methods:</b> General features, frequency allocation, properties of satellite communication systems, LEO, MEO and GEO orbits, Kepler's laws, orbital dynamics, orbital elements, Sub-satellite point, orbital perturbations, orbital effects on communication system performance. Launching and positioning of satellite. Antenna look angle determination, Sub-satellite point, limits of visibility.	8
2	<b>Space Segment (satellite subsystems) and Earth Station:</b> Attitude and orbit control system; Telemetry, tracking, command and monitoring (TTC & M); communication subsystems, antenna subsystem, power system, equipment reliability and space qualification. Different types of earth stations.	9

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3	<b>Satellite Link Design:</b> Basic transmission theory, General link design equation, system noise temperature, uplink/down link design, C/N ratio, saturation flux density, input/output back off, Effect of rain (attenuation and depolarization).	10
4	<b>Satellite Multiple Access Techniques:</b> Multiplexing and multiple access, Preassigned, demand assigned multiple access, FDMA- bandwidth-limited and power limited TWT amplifier operation; TDMA- TDMA frame structure, frame efficiency, Comparison of uplink power requirements for FDMA and TDMA. CDMA- Direct-sequence spread spectrum, m-sequence codes, spectrum spreading and despreading	8
5	<b>Introduction of various Satellite systems:</b> VSAT systems, DBS, DTH; LEO and non-Geosystems- RADARSAT, IRIDIUM, INMARSAT, ORBCOMM; Global Positioning System (GPS).	5
	Total	40

12. Suggested Books:

SL. No.	Name of Authors/Books/Publishers	Year of Publication/Reprint
	<b>Text Books:</b>	
1.	Satellite Communications/ Pratt, Bostian/ John Wiley & Sons.	2001
2.	Satellite Communications/ Dennis Roddy/ McGraw-Hill.	2000
3.	Digital Satellite Communications/ Tri T. Ha./McGraw Hill.	1999

13.	<b>Mode of Evaluation</b>	Viva / Quiz / Mid Term Lab Exam / End Term Lab Exam
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Name of Department: - Electronics and Communication Engineering

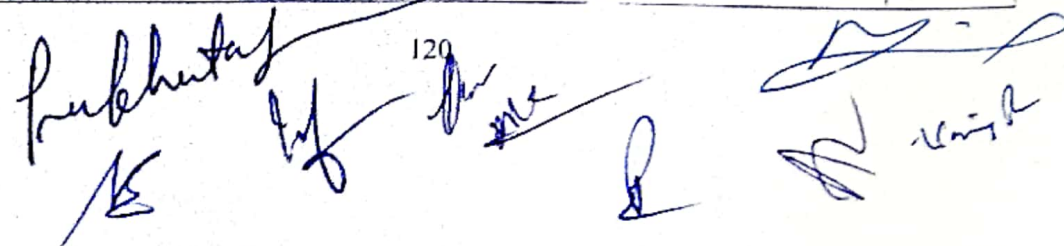
1. Subject Code: TEC821 Course Title: Neural Networks and Machine Learning
2. Contact Hours: L: 3 T: 1 P: 0
3. Examination Duration (Hrs): Theory 3 Practical 0
4. Relative Weight: CWS 25 PRS 0 MTE 25 ETE 50 PRE 0
5. Credits: 4
6. Semester: Spring (even)
7. Subject Area: Elective
8. Pre-requisite: **Basic probability theory and basic linear algebra**

<b>9. Course Outcomes:</b>	<ul style="list-style-type: none"> <li>Understand the role of neural networks in engineering, artificial intelligence, and cognitive modeling.</li> <li>Provide knowledge of supervised learning in neural networks</li> <li>Provide knowledge of computation and dynamical systems using neural networks</li> <li>Provide knowledge of reinforcement learning using neural networks.</li> <li>Provide knowledge of unsupervised learning using neural networks.</li> <li>Provide hands-on experience in selected applications .</li> </ul>
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**10. Details of the Course:**

Sl. No.	Contents	Contact Hours
1	<b>Introduction to Artificial Neural Networks:</b> Biological Neural Networks, ANN Application Overview, Pattern Analysis Tasks: Classification, Regression and Clustering, Computational Models of Neurons, Structures of Neural Networks, Learning Principles, Supervised, Unsupervised and Reinforcement Learning. <b>Linear Models of Learning and Classification:</b> Polynomial Curve Fitting, Bayesian Curve Fitting, Linear Basis Function Models, Bias-variance decomposition, Bayesian Linear Regression, Least Squares for Classification, Logistic Regression for Classification, Bayesian Logistic Regression for Classification.	12
2	<b>Feed Forward Neural Networks:</b> Pattern Classification using Perceptron, Multilayer Feed forward Neural Networks (MLFNNs), Pattern Classification using MLFNNs, Error and Back Propagation Learning, Fast Learning Methods: Conjugate Gradient Method, Auto-associative Neural Networks, Bayesian Neural Networks.	8

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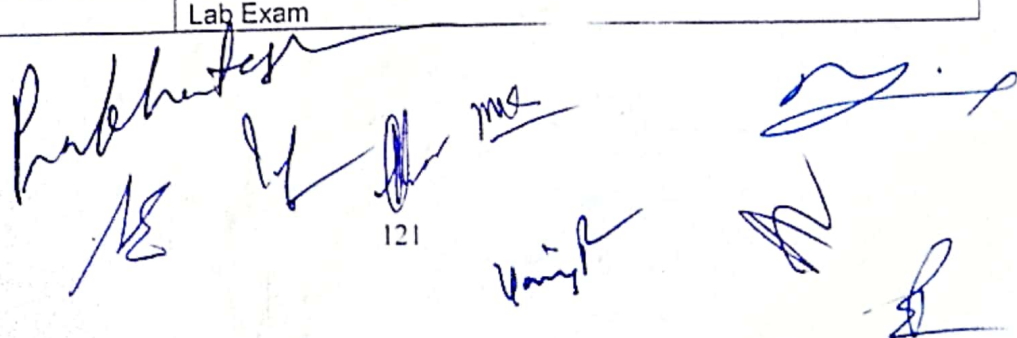


3	<b>Radial Basis Function Networks:</b> Regularization Theory, RBF networks for Function approximation, RBF networks for pattern classification.  <b>Kernel Methods for Pattern Analysis:</b> Statistical Learning Theory, Support Vector Machines for Pattern Classification, Support Vector Regression for Function Approximation, Relevance Vector Machines for Classification and Regression.	8
4	<b>Self Organizing Maps:</b> Pattern Clustering, Topological mapping, Kohonen's Self Organizing Map, Competitive Learning, Learning Vector Quantizers, Counter Propagation Networks, Adaptive Resonance Theory(ART).	6
5	<b>Feedback Neural Networks:</b> Pattern Storage and Retrieval, Hopfield Model, Boltzmann Machine, Recurrent Neural Networks.  <b>Applications of Neural Networks and Machine Learning:</b> Case Studies.	6
Total		40

#### 11. Suggested Books:

SL. No.	Name of Authors/Books/Publishers	Year of Publication/Reprint
<b>Text Books</b>		
1.	B. Yegnanarayana, Artificial Neural Networks, Prentice Hall of India.	2009
2.	Satish Kumar, Neural Networks – A Classroom Approach, Tata McGraw-Hill.	2004
<b>Reference Books</b>		
1.	S. Haykin, Neural Networks – A Comprehensive Foundation, Prentice Hall, 2E	1999
2.	C.M. Bishop, Pattern Recognition and Machine Learning, Springer, 2E	2011

12.	<b>Mode of Evaluation</b>	Test / Quiz / Assignment / Mid Term Exam / End Term Exam / Lab Exam
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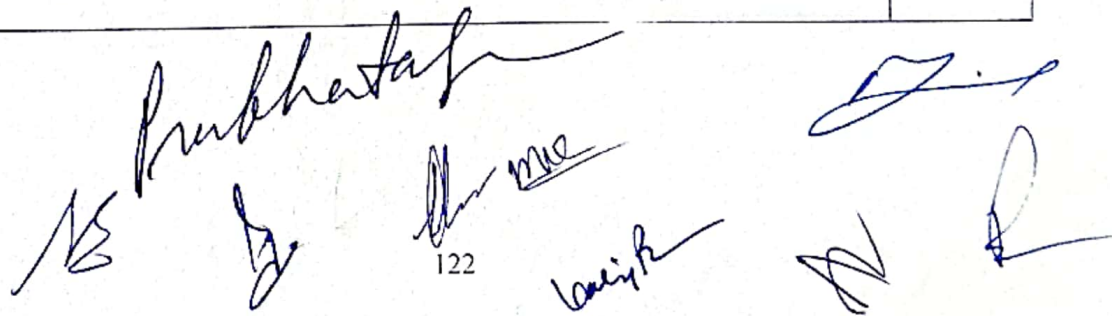
Name of Department: - **Electronics and Communication Engineering**

1. Subject Code: **TEC 822** Course Title: **Mobile Ad hoc Networks**
2. Contact Hours: L: **3** T: **1** P: **0**
3. Examination Duration (Hrs): Theory **3** Practical **0**
4. Relative Weight: CWS **25** PRS **0** MTE **25** ETE **50** PRE **0**
5. Credits: **4**
6. Semester: **Spring (Even)**
7. Subject Area: **Elective**
8. Pre-requisite: **Wireless Communication**

<b>9. Course Objectives:</b>	<ul style="list-style-type: none"> <li>Knowledge of the 802.11 Wireless LAN (WiFi), Bluetooth standards and other wireless technologies. This content of course includes their designs, operations, plus approaches to interoperability.</li> <li>This course introduces the mobile ad hoc networks, design and implementation issues, and available solutions. Understanding of MAC layer protocols and routing mechanisms and the three classes of approaches: proactive, reactive, and hybrid. Brief introduction of sensor networks and their characteristics are included.</li> <li>This course also provides the overview of energy management, security issues and quality of service in ad hoc networks.</li> </ul>
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**10. Details of the Course:**

Sl. No.	Contents	Contact Hours
1	<b>Introduction:</b> Ad hoc Networking: An Introduction. Model of operation, Symmetric links, Fundamental of wireless networks, Bluetooth, IrDA, Comparison of Bluetooth and IrDA, HomeRF, 802.11(Wi-Fi), 802.16(Wi-Max), Hotspot, Difference between cellular and ad hoc networks, Technical and research challenges, DoD perspectives.	8



2	<p><b>MAC Layer Protocols for Ad hoc wireless Networks:</b></p> <p>Need for Medium Access Control(MAC) Protocols, Issues and design goals of MAC protocols, Classification of MAC protocols: Contention Based Mac protocols, Contention Based Mac protocols with reservation mechanism, Multiple Access Collision Avoidance (MACA), Media Access Protocol for wireless (MACAW), Floor Acquisition Multiple Access Protocols (FAMA), Busy Tone Multiple Access Protocols (BTMA), Multiple Access Collision Avoidance – by Invitation(MACA-BI), Dual Busy Tone Multiple Access Protocols (DBTMA), Multichannel Carrier sense Multiple access (CSMA) MAC Protocol.</p>	10
3	<p><b>Routing Protocols:</b></p> <p>Design Issues of Routing Protocols, Ideal characteristics of Routing, Classification of Routing Protocols: Proactive, Reactive, Hybrid. Overview of DSDV( Destination Sequenced Distance Vector) Routing protocol, Link state, Distance vector, DSDV Properties an its Merits demerits, Damping Fluctuations. Clustering , Hierarchical Routing.</p> <p>Overview of DSR (Dynamic Source Routing) Protocols: DSR Properties, Additional Route Discovery and Maintenance Features. Overview of AODV (Ad Hoc On Demand Distance vector) Protocols, Unicasting ,Multicasting, Unicast Route Establishment, Multicasting Route Establishment,, Expanding Ring Search. Overview of ZRP (Zone Routing Protocol), Reconfigurable Wireless Networks, Intrazone, Interzone Routing Protocols. Overview of OLSR( Optimized Link State Routing) Protocol, Multipoint Relays (MPRs), Protocol Functioning, Core Functioning.</p>	12

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- Signature with "V" above it on the right.
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4	<b>Miscellaneous Topics:</b> Energy management System in Ad Hoc networks, Power Issues, Smart Batteries, Associativity based Routing, Effects of Beaconing of Battery Life, Maximum life Time Routing. Security in Ad Hoc wireless networks, Network Security Requirements, Issues and Challenges in Security Provisioning, Network Security Attacks. QoS in Ad Hoc wireless networks, Issues and Challenges, Classification of QoS solutions. Wireless Sensor Networks, Issues and Challenges, Sensor Network Architecture, Flooding Gossiping, Rumour Routing, Quality of Sensor Networks, Evolving Standards.	12
	<b>Total</b>	<b>42</b>

11. Suggested Books:

SL. No.	Name of Authors/Books/Publishers	Year of Publication/Reprint
<b>Text Books</b>		
1.	Perkins, C., 'Ad Hoc Networking', Addison Wesley.	2000
2.	Murthy, C. Siva Ram, and Manoj, B. S., 'Ad Hoc Wireless Networks Architecture and Protocols', Pearson Education 2 <sup>nd</sup> Edition.	2004
<b>Reference Books</b>		
1.	Basagni, S. And Conti M., 'Mobile Ad Hoc Networking', Wiley,	2004

12.	<b>Mode of Evaluation</b>	Test / Quiz / Assignment / Mid Term Exam / End Term Exam / Lab Exam
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Name of Department: - Electronics and Communication Engineering

1. Subject Code:  Course Title:
2. Contact Hours: L:  T:  P:
3. Examination Duration (Hrs): Theory  Practical
4. Relative Weight: CWS  PRS  MTE  ETE  PRE
5. Credits:
6. Semester:
7. Subject Area:
8. Pre-requisite: Digital Electronics, Computer Organization, Microprocessor Fundamentals

9. Course Objectives:	The course aims to introduce the student to the detailed design and analysis of computer and microprocessor architectures.
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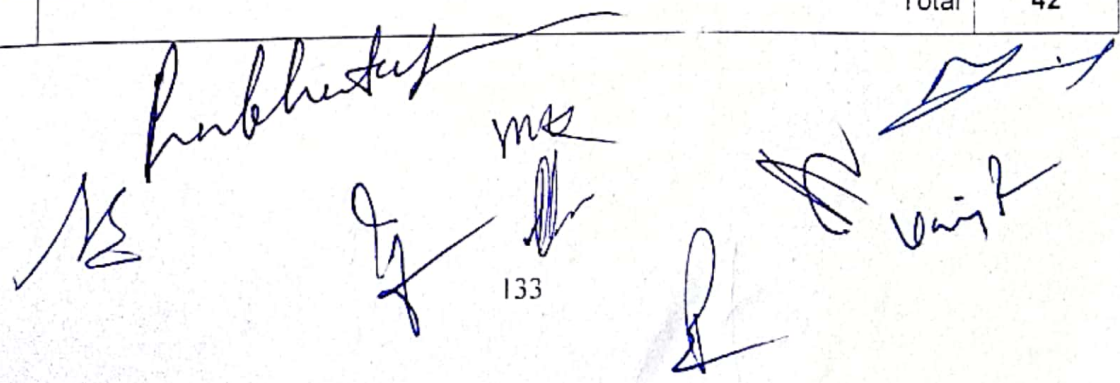
10. Details of the Course:

Sl. No.	Contents	Contact Hours
1	<p><b>Review of Digital Logic Circuits:</b> Logic Gates, Boolean Algebra, Map Simplification, Combinational Circuits, Flip-Flops, Sequential Circuits,</p> <p><b>Review of Digital Components:</b> Decoders, Multiplexors, Registers, Shift Registers, Counters, Memory Units</p> <p><b>Review of Data Representation:</b> Data Types, Complements, Fixed Point Representation, Floating Point Representation, Other Binary Codes, Error Detection Codes.</p> <p><b>Computer Arithmetic:</b> Addition and Subtraction, Multiplication Algorithms, Division Algorithms, Floating Point Arithmetic Operations, Decimal Arithmetic Unit, Decimal Arithmetic Operations.</p>	9
2	<p><b>Register Transfer and Microoperations:</b> Register Transfer Language, Register Transfer, Bus and Memory</p>	8

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	<p>Transfers, Arithmetic Microoperations, Logic Microoperations, Shift Microoperations, Arithmetic Logic Shift Unit, Hardware Description Languages.</p> <p><b>Basic Computer Organization and Design:</b>  Instruction Codes, Computer Registers, Computer Instructions, Timing and Control, Instruction Cycle, Memory Reference Instructions, Input Output and Interrupt, Complete Computer Description, Design of a Basic Computer, Design of Accumulator Logic.</p> <p><b>Programming the Basic Computer:</b>  Machine Language, Assembly Language, The Assembler, Program Loops, Programming Arithmetic and Logic Operations, Subroutines, Input-Output Programming.</p>	
3	<p><b>Microprogrammed Control:</b>  Control Memory, Address Sequencing, Microprogram Example, Design of Control Unit.</p> <p><b>Central Processing Unit:</b>  General Register Organization, Stack Organization, Instruction Formats, Addressing Modes, Data Transfer and Manipulation, Program Control, Reduced Instruction Set Computer (RISC).</p>	9
4	<p><b>Pipeline and Vector Processing:</b>  Parallel Processing, Pipelining, Arithmetic Pipeline, Instruction Pipeline, RISC Pipeline, Vector Processing, Array Processors.</p> <p><b>Input Output Organization:</b>  Peripheral Devices, Input Output Interface, Asynchronous Data Transfer, Modes of Transfer, Priority Interrupt, Direct Memory Access, Input Output Processor, Serial Communication.</p>	8
5	<p><b>Memory Organization:</b>  Memory Hierarchy, Main Memory, Auxiliary Memory, Associative Memory, Cache Memory, Virtual Memory, Memory Management Hardware.</p> <p><b>Multiprocessors:</b>  Characteristics of Multiprocessors, Interconnection Structures, Interprocessor Arbitration, Interprocessor Communication and Synchronization.</p>	8
	Total	42


  
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11. Suggested Books:

SL. No.	Name of Authors/Books/Publishers	Year of Publication/Reprint
<b>Text Books</b>		
1.	M. Morris Mano: Computer System Architecture, 3 <sup>rd</sup> Edition, Pearson Education.	2013
2.	Linda Null, Julia Lobur: Essentials of Computer Organization and Architecture, 4 <sup>th</sup> Edition, Jones and Bartlett Publishers.	2003
<b>Reference Books</b>		
1.	David A. Patterson, John L. Hennessy: Computer Organization and Design – The Hardware / Software Interface, 3 <sup>rd</sup> Edition, Morgan Kaufman.	2005
2.	William Stallings: Computer Organization & Architecture, 8th Edition, PHI.	2010
12.	<b>Mode of Evaluation</b>	Test / Quiz / Assignment / Mid Term Exam / End Term Exam / Lab Exam

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## GRAPHIC ERA UNIVERSITY DEHRADUN

Name of Department: - Electronics and Communication Engineering

1. Subject Code: TEC 834 Course Title: Testing of VLSI Circuits
2. Contact Hours: L: 3 T: 1 P: 0
3. Examination Duration (Hrs): Theory 3 Practical 0
4. Relative Weight: CWS 25 PRS 0 MTE 25 ETE 50 PRE 0
5. Credits: 4
6. Semester: Spring (Even)
7. Subject Area: Elective
8. Pre-requisite

<b>9. Course Outcomes:</b>	<ul style="list-style-type: none"> <li>The course will impart the knowledge about the basic of VLSI testing. The different fault models and logic and fault simulations</li> <li>The course covers the testability SCOPES for the combinational circuits and memory testing.</li> <li>Along with it the discussion about the fundamental of the Logic testing and embedded core testing are included.</li> </ul>
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**11. Details of the Course:**

Sl. No.	Contents	Contact Hours
1	<p><b>Introduction:</b> Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends Affecting Testing.</p> <p><b>Fault Modeling:</b> Defects, Errors, and Faults, Functional Versus Structural Testing, Levels of Fault Models, A Glossary of Fault Models, Single Stuck-at Fault.</p> <p><b>Logic and Fault Simulation:</b> Simulation for Design Verification, Simulation for Test Evaluation, Modeling Circuits for Simulation</p>	9
2	<p><b>Testability Measures:</b> SCOAP Controllability and Observability, High-Level Testability Measures.</p> <p><b>Combinational Circuit Test Generation:</b> Algorithms and Representations, Redundancy Identification (RID), Testing as a Global Problem, Definitions, Test Generation Systems, Test</p>	8

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	Compaction, Significant Combinational ATPG Algorithms and sequential circuit test generation.	
3	<b>Memory Test:</b> Memory Density and Defect Trends, Faults, Memory Test Levels, March Test Notation, Fault Modeling, Memory Testing, Analog and Mixed Signal Test, Delay Test and IDDQ test.	9
4	<b>Fundamental Techniques for Logic Testing:</b> Design For Test fundamentals, ATPG fundamental, scan architecture and technique.	8
5	<b>Embedded Core Test Fundamentals:</b> Introduction to Embedded Core Testing, Core, Core-Based Design, Core DFT Development, Chip Design with a Core, Scan Testing the Isolated Core, Scan Testing the Non-Core Logic, User Defined Logic Chip-Level DFT Concerns, Memory Testing with BIST.	8
	Total	42

11. Suggested Books:

SL. No.	Name of Authors/Books/Publishers	Year of Publication/Reprint
	<b>Text Books</b>	
1.	Viswani D. Agarwal Michael L. Bushnell, <i>Essentials of electronic testing for digital memory &amp; mixed signal VLSI circuit</i> , Kluwer Academic Publications.	1999
2.	Alfred L. Crouch, <i>Design for test for digital IC's and embedded core systems</i> , PHI.	1999
	<b>Reference Books</b>	
1.	Parag. K. Lala, <i>Digital circuit testing and testability</i> , Academic Press.	1997

12.	<b>Mode of Evaluation</b>	Test / Quiz / Assignment / Mid Term Exam / End Term Exam / Lab Exam
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